1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2011-02-08

K60 MLB

LAST_MODIFIED=Tue Feb 8 14:39:56 2011

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ABBREV=DRAWING
LAST_MODIFIED=Tue Feb 8 14:39:56 2011

DRAWING TITLE: SCH,K60,MLB

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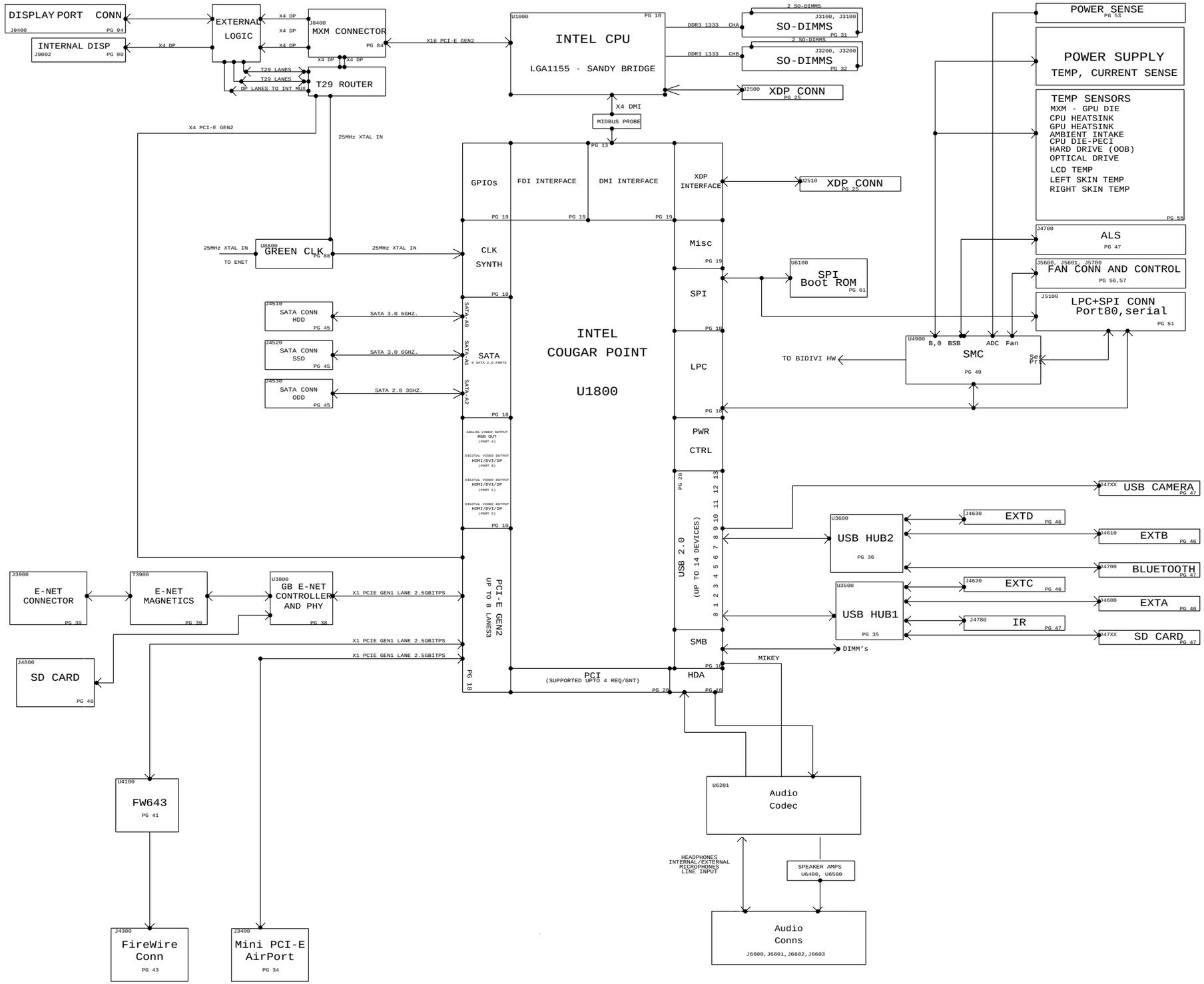

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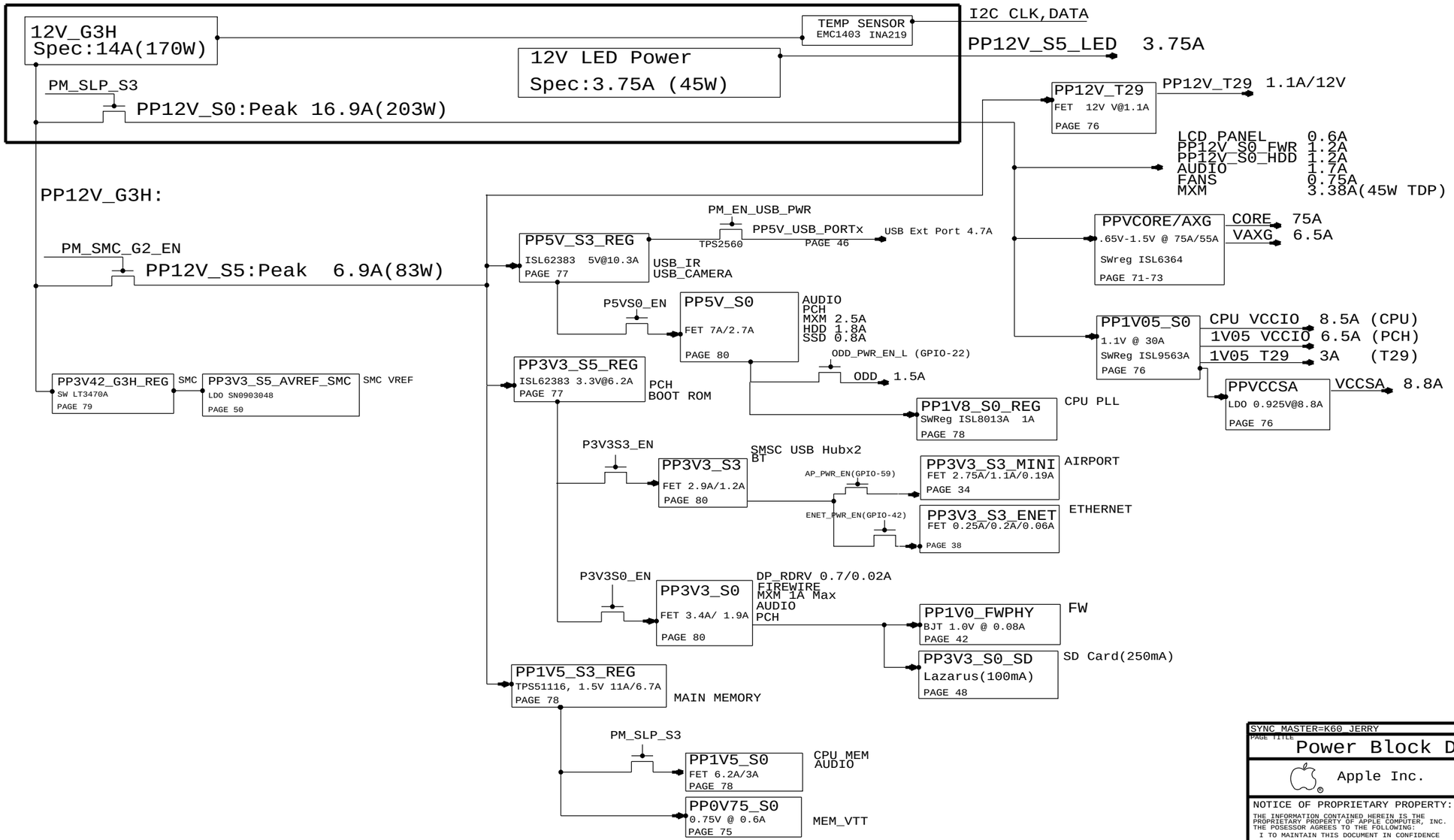
AC/DC POWER SUPPLY (Spec:215W)



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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-0801	PCBA,MLB,DEV,K60	DEVELOPMENT,DEV_GROUP
639-1767	PCBA,MLB,K60,2.5G,4C,PRQ,P2_ODD	K60,2P5GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,YES_DBG
639-1820	PCBA,MLB,K60,2.7G,4C,PRQ,P2_ODD	K60,2P7GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,YES_DBG
639-1821	PCBA,MLB,K60,2.8G,4C,PRQ,P2_ODD	K60,2P8GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,YES_DBG
639-2160	PCBA,MLB,K60,2.5G,4C,PRQ,P2_ODD,NO_DBG	K60,2P5GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,NO_DBG
639-2159	PCBA,MLB,K60,2.7G,4C,PRQ,P2_ODD,NO_DBG	K60,2P7GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,NO_DBG
639-2161	PCBA,MLB,K60,2.8G,4C,PRQ,P2_ODD,NO_DBG	K60,2P8GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,NO_DBG
639-2118	PCBA,MLB,K60,2.5G,4C,PRQ,P1_ODD	K60,2P5GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,YES_DBG
639-2122	PCBA,MLB,K60,2.7G,4C,PRQ,P1_ODD	K60,2P7GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,YES_DBG
639-2119	PCBA,MLB,K60,2.8G,4C,PRQ,P1_ODD	K60,2P8GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,YES_DBG
639-2132	PCBA,MLB,K60,2.5G,4C,PRQ,P1_ODD,NO_DBG	K60,2P5GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,NO_DBG
639-2133	PCBA,MLB,K60,2.7G,4C,PRQ,P1_ODD,NO_DBG	K60,2P7GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,NO_DBG
639-2134	PCBA,MLB,K60,2.8G,4C,PRQ,P1_ODD,NO_DBG	K60,2P8GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,NO_DBG

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC1	COMMON,ALTERNATE,MXM,FCIM,CPU_1V5_SENSE,CPU_VCCSA_SENSE,1V05_PCH_SENSE,HUB_USX2061,PRODUCTION,VAXG,SSD
BASIC2	AP,BT,IR,T29
DEV_GROUP	VREFMRGN_A,VREFMRGN_B,DIMM_1V5_SENSE
YES_DBG	XDP,XDP_CONN,XDP_CPU_BPM,MOJOMUX:YES,LPCPLUS:YES
NO_DBG	MOJOMUX:NO,LPCPLUS:NO

CPU SOCKET & ILM SUB-BOMS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0071	1	SOCKET,LGA1155,CPU-LF	U1000	CRITICAL	TYCO_SOCKET
604-1474	1	ASSY,PURCHASED,ILM,TYCO	ILM	CRITICAL	TYCO_SOCKET
511S0073	1	SOCKET,LGA1155,CPU-LF	U1000	CRITICAL	MOLEX_SOCKET
604-1161	1	ASSY,PURCHASED,ILM,MOLEX	ILM	CRITICAL	MOLEX_SOCKET

BOM NUMBER	BOM NAME	BOM OPTIONS
085-2452	SUB ASSY,CPU SOCKET,K60,TYCO	TYCO_SOCKET
085-2453	SUB ASSY,CPU SOCKET,K60,MOLEX	MOLEX_SOCKET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
085-2452	1	TYCO CPU SOCKET AND ILM	SKT_ILM	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
085-2453	085-2452		SKT_ILM	MOLEX ALTERNATE

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

COMMON

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	337S4088	1	IC,COUGAR POINT,SLJ4F,BD82Z68,PRQ,B3	U1800	CRITICAL	
	353S3055	1	IC,PI3VEDP212,X2 DP MUX,QFN	U9390	CRITICAL	
	338S0753	1	IC,FW643,1394B_PCIE,PHY/LINK	U4100	CRITICAL	
	825-7122	1	MLB LABEL,48.0X4.8	X14	CRITICAL	
	343S0534	1	IC,BCM57765,ENET&SD,8X8	U3900	CRITICAL	
RAW: 335S0807	341T0184	1	FLASH,EFI BOOTROM,K60/K62	U6100	CRITICAL	
RAW: 335S0539	341T0328	1	SFLASH ENET 2MBIT,CIV	U3990	CRITICAL	
	338S0945	1	T29 ROUTER, IC ASSP	U9700	CRITICAL	T29
RAW: 335S0550	341T0257	1	IC,T29,SERIAL EEPROM	U9790	CRITICAL	T29
RAW: 337S3997	341T0326	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29
RAW: 335S0709	341T0330	1	IC,MXM SYS ROM,24C02	U8570	CRITICAL	
RAW: 338S0878	341T0185	1	IC,SMC,K60	U4900	CRITICAL	K60

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4043	1	SNB,SR00S,PRQ,D2,2.5,65W,4+1,6M,LGA	CPU	CRITICAL	2P5GHZ_SNB_CPU_PRQ
337S4062	1	SNB,SR009,PRQ,D2,2.7,65W,4+1,6M,LGA	CPU	CRITICAL	2P7GHZ_SNB_CPU_PRQ
337S4061	1	SNB,SR00E,PRQ,D2,2.8,65W,4+1,8M,LGA	CPU	CRITICAL	2P8GHZ_SNB_CPU_PRQ

K60 PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-8115	1	SCH,MLB,K60	SCH1		K60
820-2641	1	PCBF,MLB,K60	MLB1		K60

K60 ALTERNATE PARTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0298	128S0293			330UF
371S0679	371S0652			PIN DIODE
377S0107	377S0066			USB DIODE
376S0972	376S0612			ROHM TRA-BJT

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BOM Configuration

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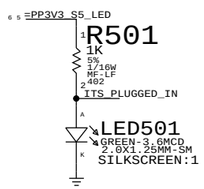
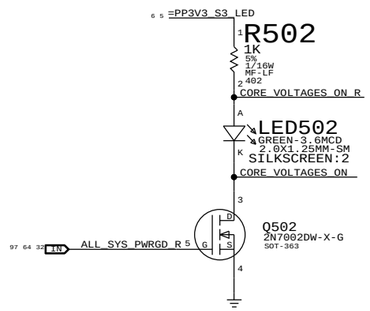
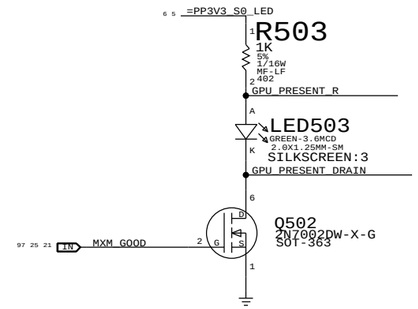
S5 Led



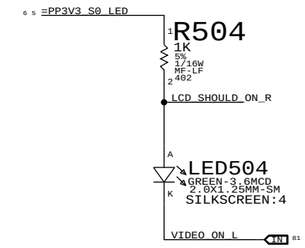
ALL_SYS_PWRGD Led



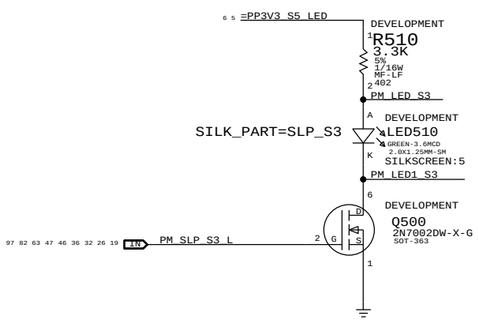
MXM PWR GOOD Led

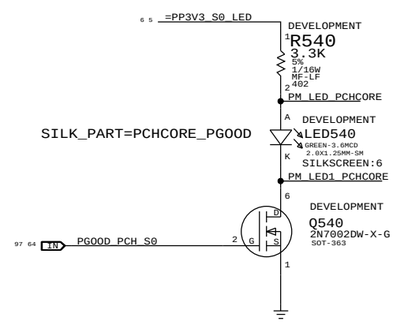


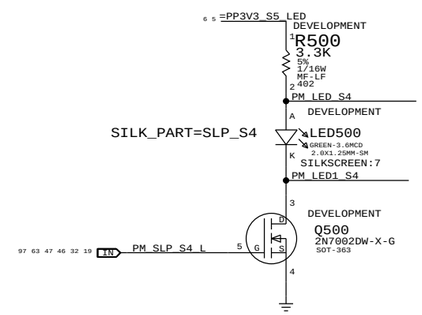
VIDEO ON Led

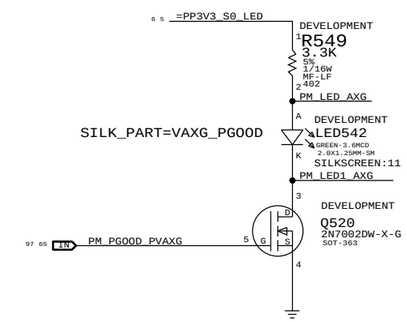


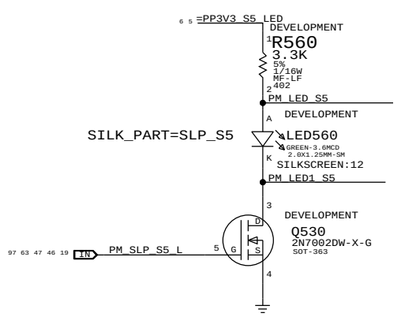
PROTO DEBUG LEDS ARE SHOWN BELOW

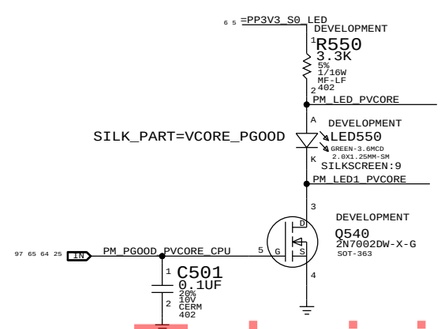


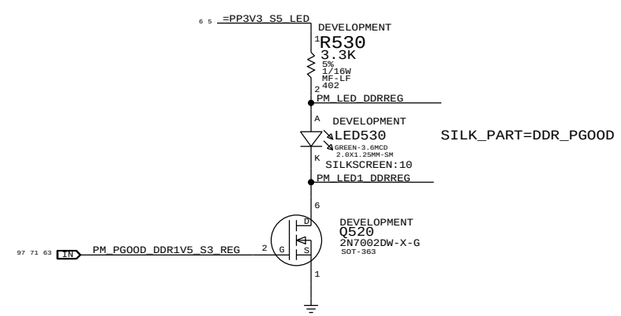


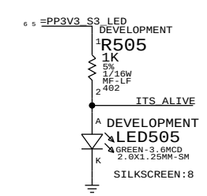












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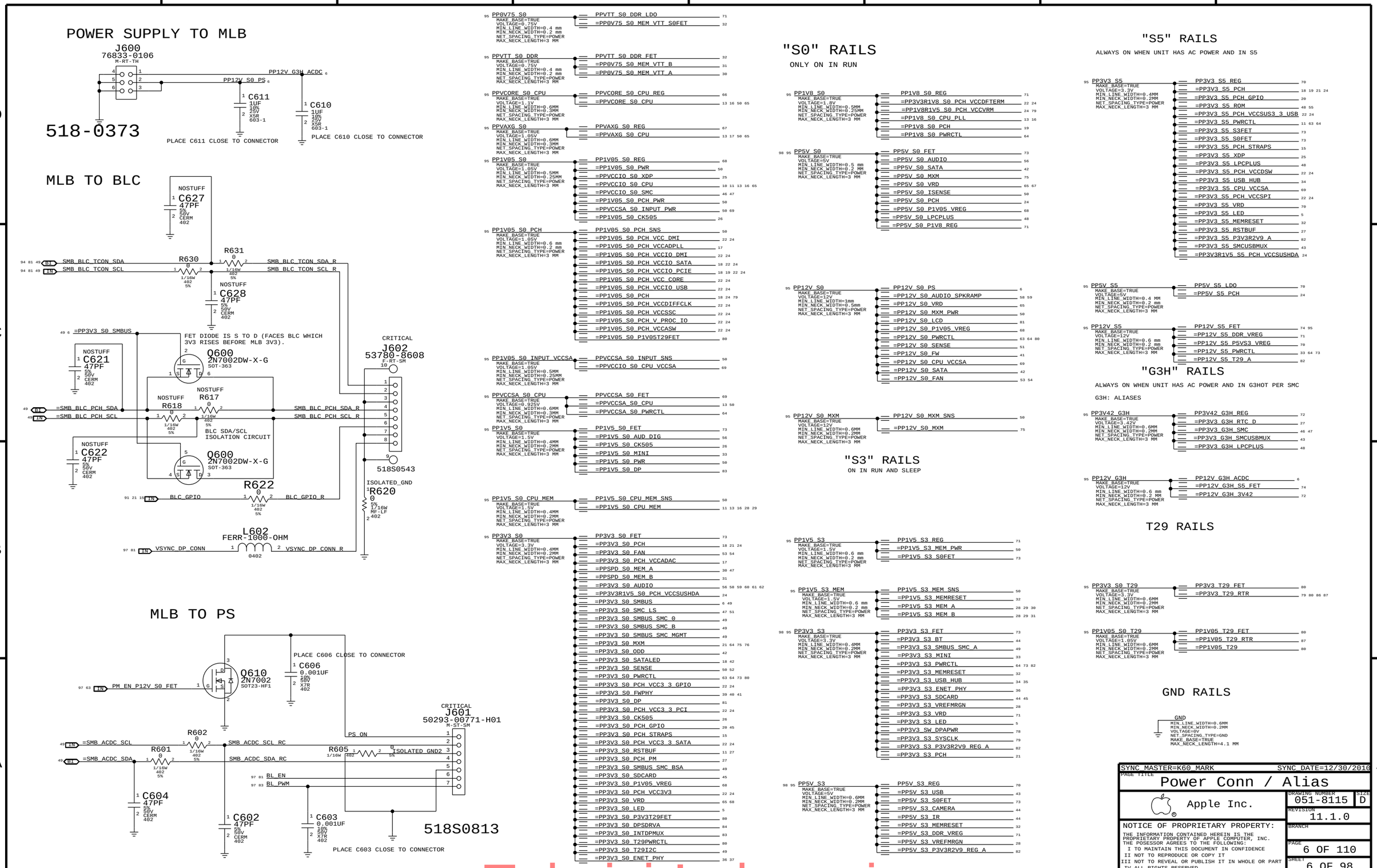

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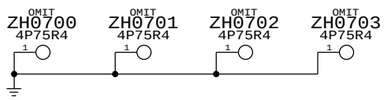
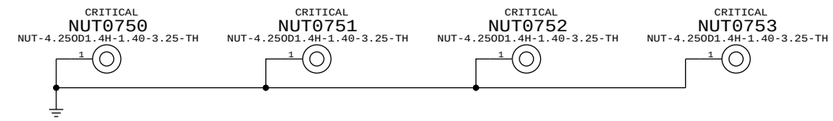
CPU Heatsink

4mm Plated Holes (998-0850)



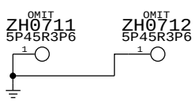
DIMM CONNECTOR NUTS

Nuts (805-9582)



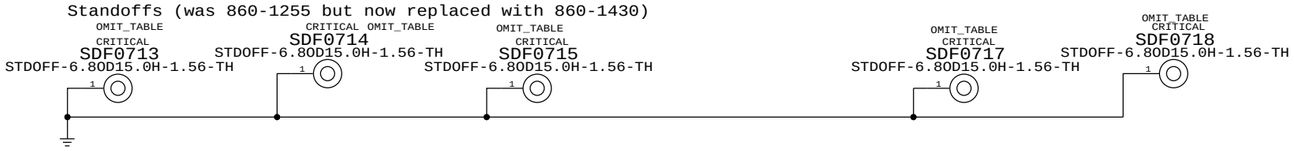
PCH HEATSINK

MOUNTING HOLES (998-0873, 998-0976)



Rear Cover

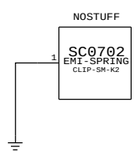
Standoffs (was 860-1255 but now replaced with 860-1430)



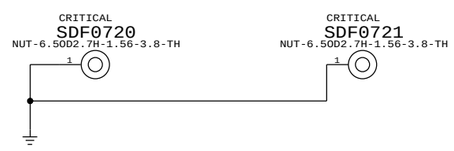
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
860-1430	5	STANDOFF,MLB,K60/K62	SDF0713,SDF0714,SDF0715,SDF0717,SDF0718	

For EMC

EMC Spring (870-1577); Near DIMMs



MXM STANDOFFS (835-0272)



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PAGE TITLE: Holes

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UNUSED CPU SIGNALS

10	TP_CPU_RSVD<16..1>	NC_CPU_RSVD<16..1>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_RSVD<46..19>	NC_CPU_RSVD<46..19>	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED PCI ALIASES

20	TP_PCI_AD<31..0>	NC_PCI_AD<31..0>	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_C_BE_L<3..0>	NC_PCI_C_BE_L<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_PAR	NC_PCI_PAR	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_RESET_L	NC_PCI_RESET_L	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_LPC_DREQ0_L	NC_LPC_DREQ0_L	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED MEM ALIASES

12	TP_MEM_A_DQ_CB<7..0>	NC_MEM_A_DQ_CB<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_A_DQS_N<8>	NC_MEM_A_DQSN<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_A_DQS_P<8>	NC_MEM_A_DQSP<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQ_CB<7..0>	NC_MEM_B_DQ_CB<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQS_N<8>	NC_MEM_B_DQSN<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQS_P<8>	NC_MEM_B_DQSP<8>	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED MISC ALIASES

18	TP_HDA_SDIN1	NC_HDA_SDIN1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_HDA_SDIN2	NC_HDA_SDIN2	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_HDA_SDIN3	NC_HDA_SDIN3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM0	NC_PCH_PWM0	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM1	NC_PCH_PWM1	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM2	NC_PCH_PWM2	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM3	NC_PCH_PWM3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_SST	NC_PCH_SST	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_CLK1	NC_PCH_CL_CLK1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_DATA1	NC_PCH_CL_DATA1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_RST1	NC_PCH_CL_RST1	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED PCIE ALIASES

18	TP_PCIE_CLK100M_PE5P	NC_PCIE_CLK100M_PE5P	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE5N	NC_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE6P	NC_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE6N	NC_PCIE_CLK100M_PE6N	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE7P	NC_PCIE_CLK100M_PE7P	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE7N	NC_PCIE_CLK100M_PE7N	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_RX_N<3..0>	NC_PE_RXN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_RX_P<3..0>	NC_PE_RXP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_TX_N<3..0>	NC_PE_TXN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_TX_P<3..0>	NC_PE_TXP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_D2R_PERN4	NC_PCIE_D2R_PERN4	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_D2R_PERP4	NC_PCIE_D2R_PERP4	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_R2D_PETN4	NC_PCIE_R2D_PETN4	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_R2D_PETP4	NC_PCIE_R2D_PETP4	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE4P	NC_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE4N	NC_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED USB ALIASES

20	TP_USB_1N	NC_USB_1N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_1P	NC_USB_1P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_2N	NC_USB_2N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_2P	NC_USB_2P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_3N	NC_USB_3N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_3P	NC_USB_3P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_4N	NC_USB_4N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_4P	NC_USB_4P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_5N	NC_USB_5N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_5P	NC_USB_5P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_6N	NC_USB_6N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_6P	NC_USB_6P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_7N	NC_USB_7N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_7P	NC_USB_7P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_10N	NC_USB_10N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_10P	NC_USB_10P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_11N	NC_USB_11N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_11P	NC_USB_11P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_12N	NC_USB_12N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_12P	NC_USB_12P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_13N	NC_USB_13N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_13P	NC_USB_13P	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED DISPLAY ALIASES

19	TP_CRT_IG_DDC_CLK	NC_CRT_IG_DDC_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_DDC_DATA	NC_CRT_IG_DDC_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_RED	NC_CRT_IG_RED	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_GREEN	NC_CRT_IG_GREEN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_BLUE	NC_CRT_IG_BLUE	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_HSYNC	NC_CRT_IG_HSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_VSYNC	NC_CRT_IG_VSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_MLN<3..0>	NC_DP_IG_B_MLN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_MLP<3..0>	NC_DP_IG_B_MLP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_AUX_N	NC_DP_IG_B_AUXN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_AUX_P	NC_DP_IG_B_AUXP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_HPD	NC_DP_IG_B_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_DDC_CLK	NC_DP_IG_B_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_DDC_DATA	NC_DP_IG_B_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_MLN<3..0>	NC_DP_IG_C_MLN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_MLP<3..0>	NC_DP_IG_C_MLP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_AUX_N	NC_DP_IG_C_AUXN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_AUX_P	NC_DP_IG_C_AUXP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_HPD	NC_DP_IG_C_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_CTRL_CLK	NC_DP_IG_C_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_CTRL_DATA	NC_DP_IG_C_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_MLN<3..0>	NC_DP_IG_D_MLN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_MLP<3..0>	NC_DP_IG_D_MLP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_AUXN	NC_DP_IG_D_AUXN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_AUXP	NC_DP_IG_D_AUXP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_HPD	NC_DP_IG_D_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_CTRL_CLK	NC_DP_IG_D_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_CTRL_DATA	NC_DP_IG_D_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_TVCLKINN	NC_SDVO_TVCLKINN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_TVCLKINP	NC_SDVO_TVCLKINP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_STALLN	NC_SDVO_STALLN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_STALLP	NC_SDVO_STALLP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_INTN	NC_SDVO_INTN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_INTP	NC_SDVO_INTP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_BKLTCTL	NC_PCH_L_BKLTCTL	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_BKLTEN	NC_PCH_L_BKLTEN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_VDD_EN	NC_PCH_L_VDD_EN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CLKOUT_DPN	NC_PCH_CLKOUT_DPN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CLKOUT_DPP	NC_PCH_CLKOUT_DPP	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED FDI ALIASES

10	TP_CPU_FDI_TX_N<7..0>	NC_CPU_FDI_TXN<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_FDI_TX_P<7..0>	NC_CPU_FDI_TXP<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_FDI_RX_N<7..0>	NC_PCH_FDI_RXN<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_FDI_RX_P<7..0>	NC_PCH_FDI_RXP<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED SATA ALIASES

19	TP_SATA_D_D2RN	NC_SATA_D_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SATA_D_D2RP	NC_SATA_D_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SATA_D_R2D_CN	NC_SATA_D_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SATA_D_R2D_CP	NC_SATA_D_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SATA_E_D2RN	NC_SATA_E_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SATA_E_D2RP	NC_SATA_E_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SATA_E_R2D_CN	NC_SATA_E_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SATA_E_R2D_CP	NC_SATA_E_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SATA_F_D2RN	NC_SATA_F_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SATA_F_D2RP	NC_SATA_F_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SATA_F_R2D_CN	NC_SATA_F_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SATA_F_R2D_CP	NC_SATA_F_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
UNUSED SIGNAL ALIAS

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PEG Slot Support

THIS SIGNAL NAME IS CONNECTED TO MXM

18 IN	PEG_CLK100M_P	90	GPU_CLK100M_PCIE_P (MAKE_BASE=TRUE)	CLK_100M_MXM_P OUT 75
18 IN	PEG_CLK100M_N	90	GPU_CLK100M_PCIE_N (MAKE_BASE=TRUE)	CLK_100M_MXM_N OUT 75
19 IN	=PEG_R2D_C_P<0..15>		PEG_R2D_C_P<0..15> (MAKE_BASE=TRUE)	OUT 77 90
19 IN	=PEG_R2D_C_N<0..15>		PEG_R2D_C_N<0..15> (MAKE_BASE=TRUE)	OUT 77 90
19 OUT	=PEG_D2R_P<0..15>		PEG_D2R_P<0..15> (MAKE_BASE=TRUE)	IN 77 90
19 OUT	=PEG_D2R_N<0..15>		PEG_D2R_N<0..15> (MAKE_BASE=TRUE)	IN 77 90
21 IN	PEG_CLKREQ_L		MXM_CLKREQ_L (MAKE_BASE=TRUE)	OUT 75 97
75	MXM_RESET_L		PEG_RESET_L (MAKE_BASE=TRUE)	27 97

97 91 19 IN PM_CLK32K_SUSCLK_R — R929 22 5% 1/16W MF-LF 402 (1, 2) — PM_CLK32K_SUSCLK OUT 46 91 97

PLACEMENT_NOTE=PLACE CLOSE TO U1800

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PAGE TITLE
Signal Aliases

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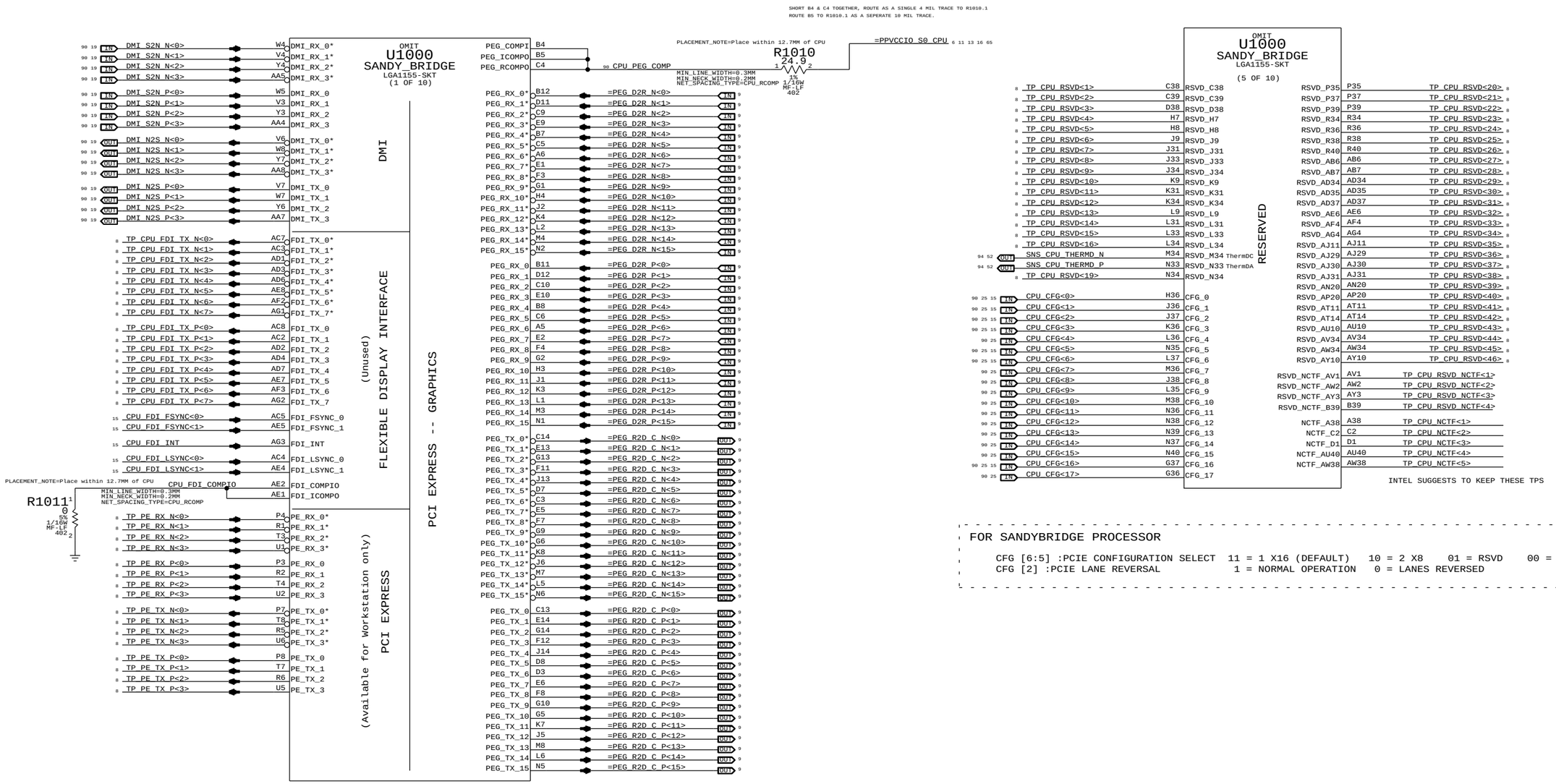

FOR SANDYBRIDGE PROCESSOR

CFG [6:5] :PCIE CONFIGURATION SELECT 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [2] :PCIE LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

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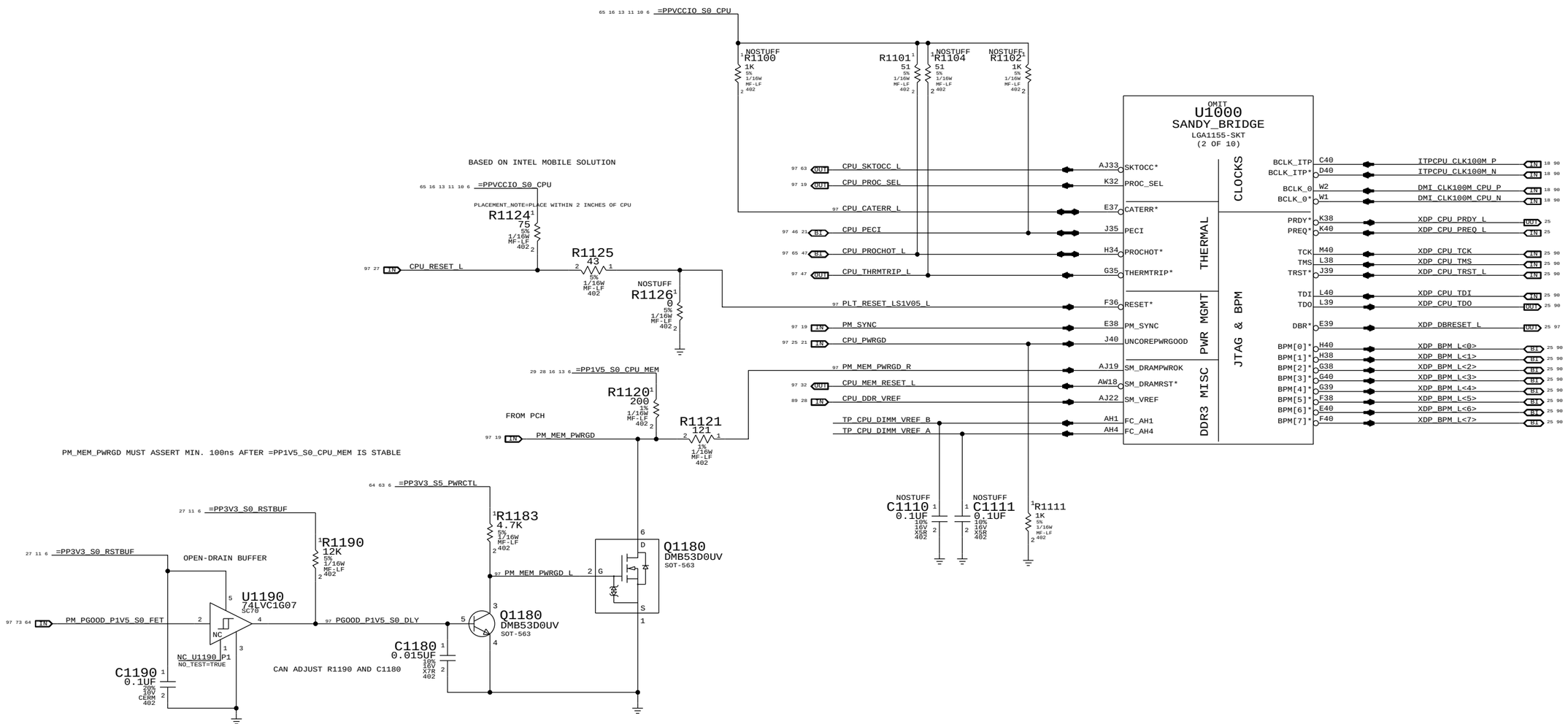

PAGE TITLE
CPU CLOCK/MISC/JTAG

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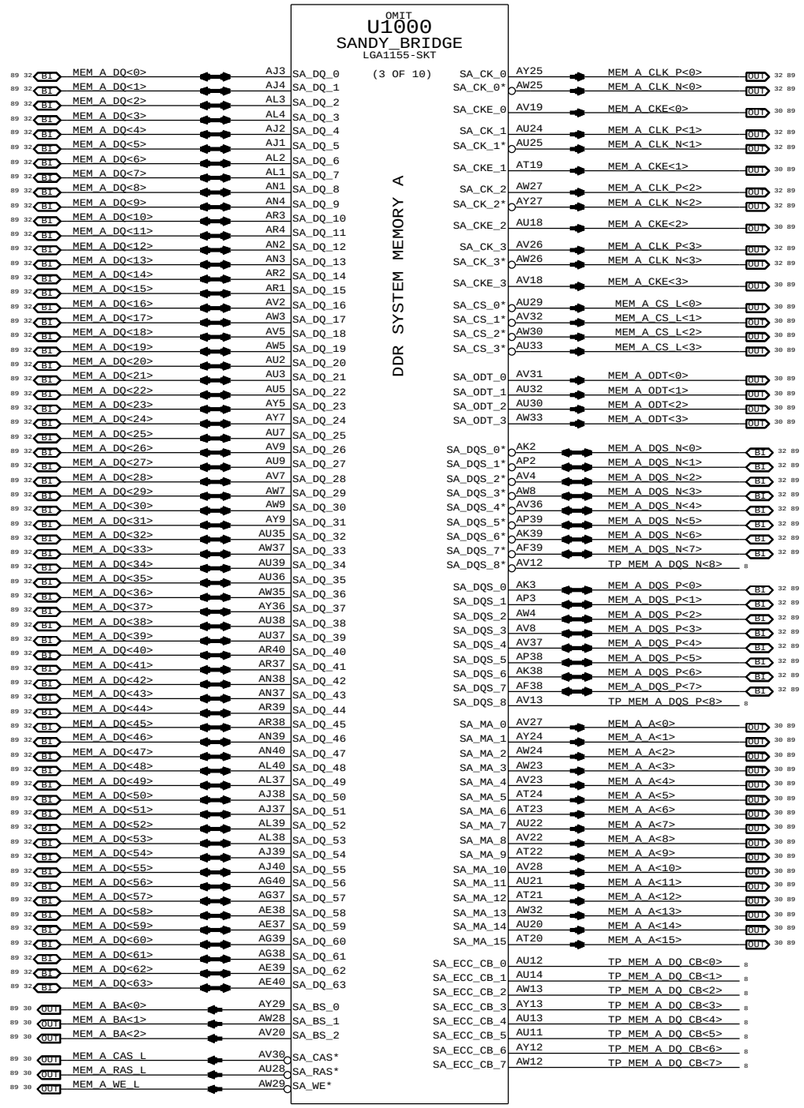

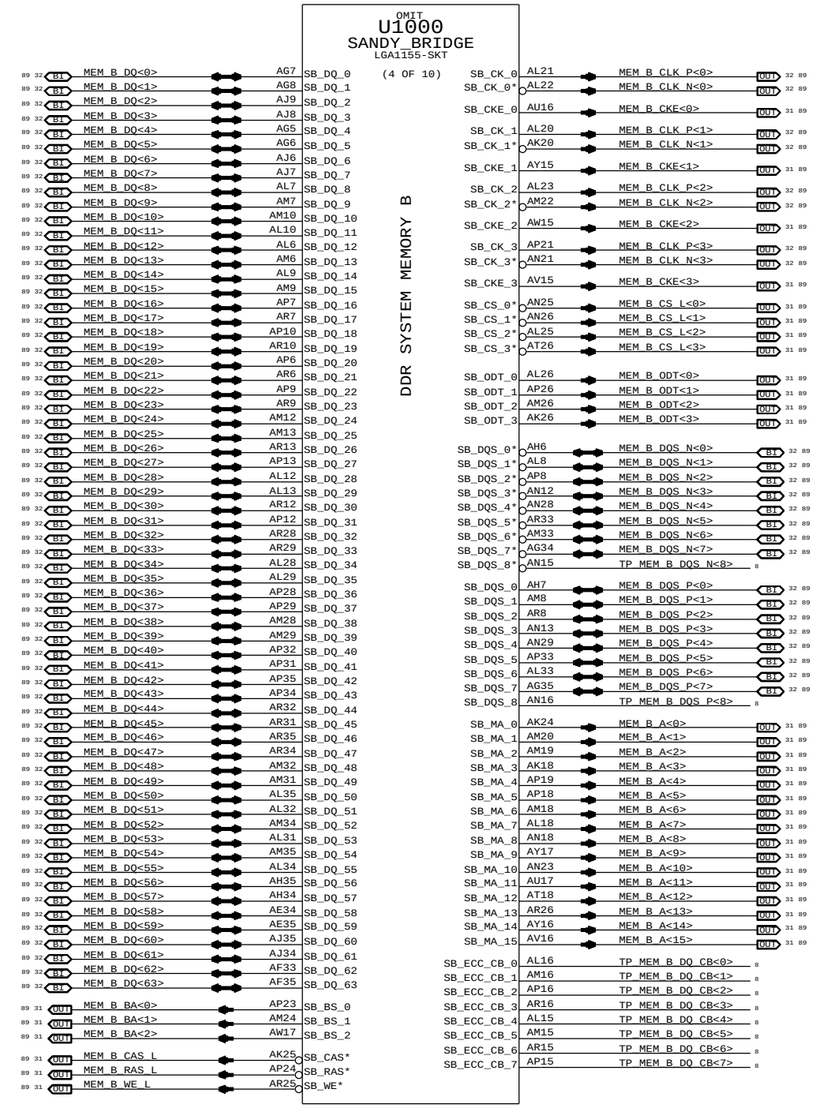

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PAGE TITLE
CPU DDR3 INTERFACES

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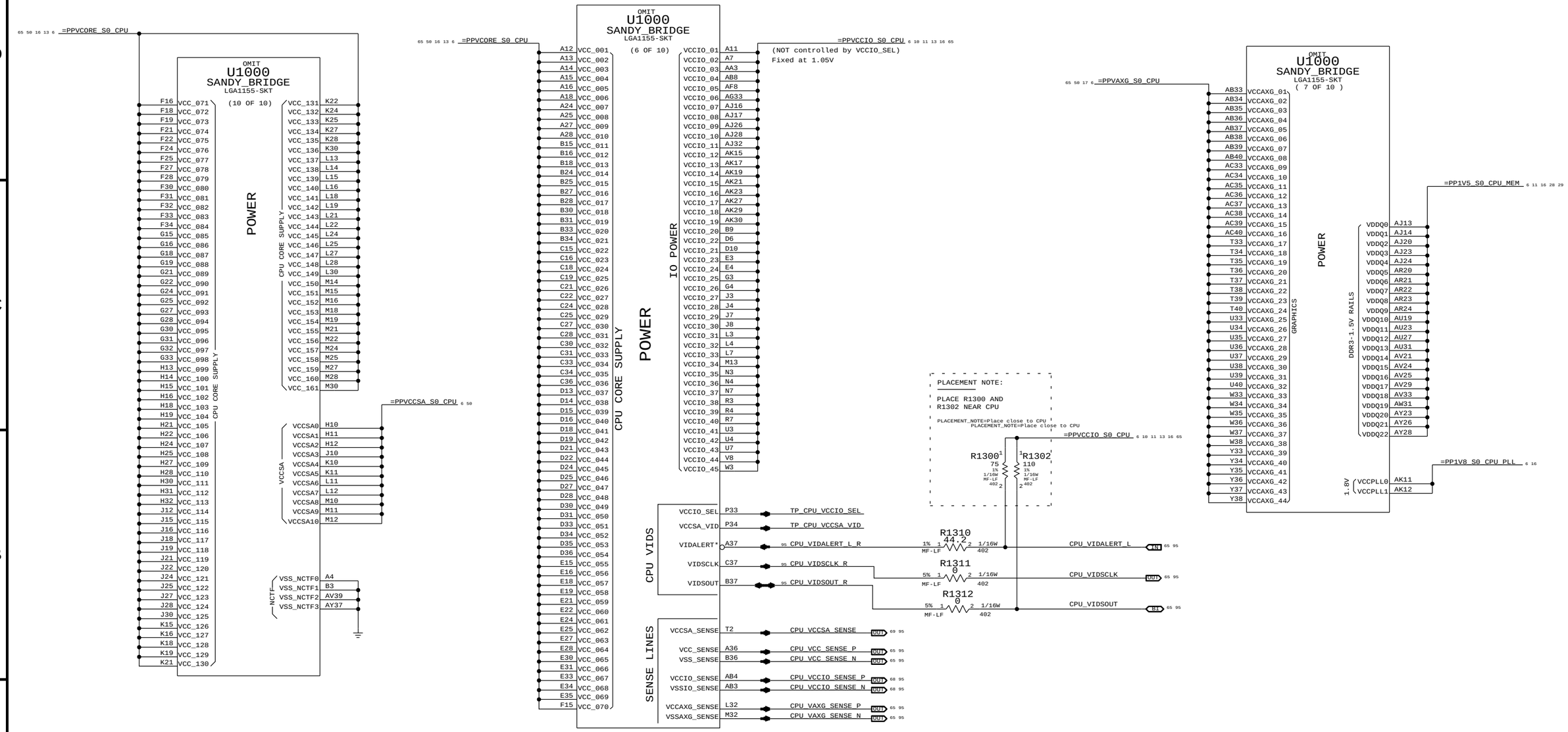

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
CPU POWER

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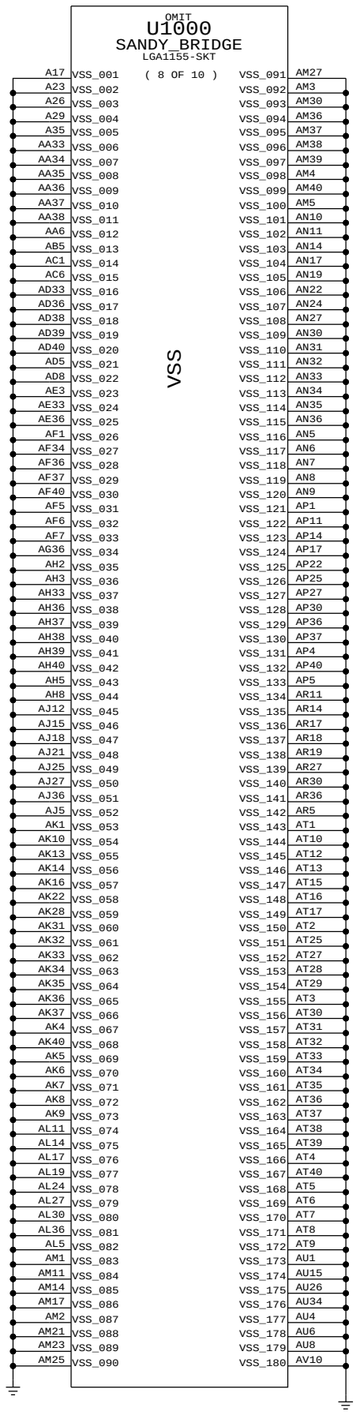

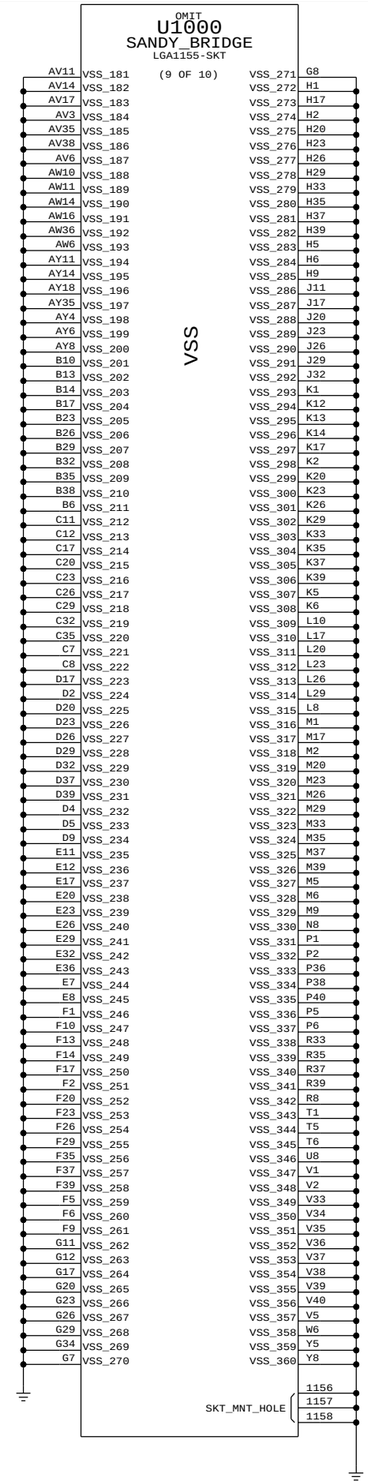

PAGE TITLE

CPU GROUNDS

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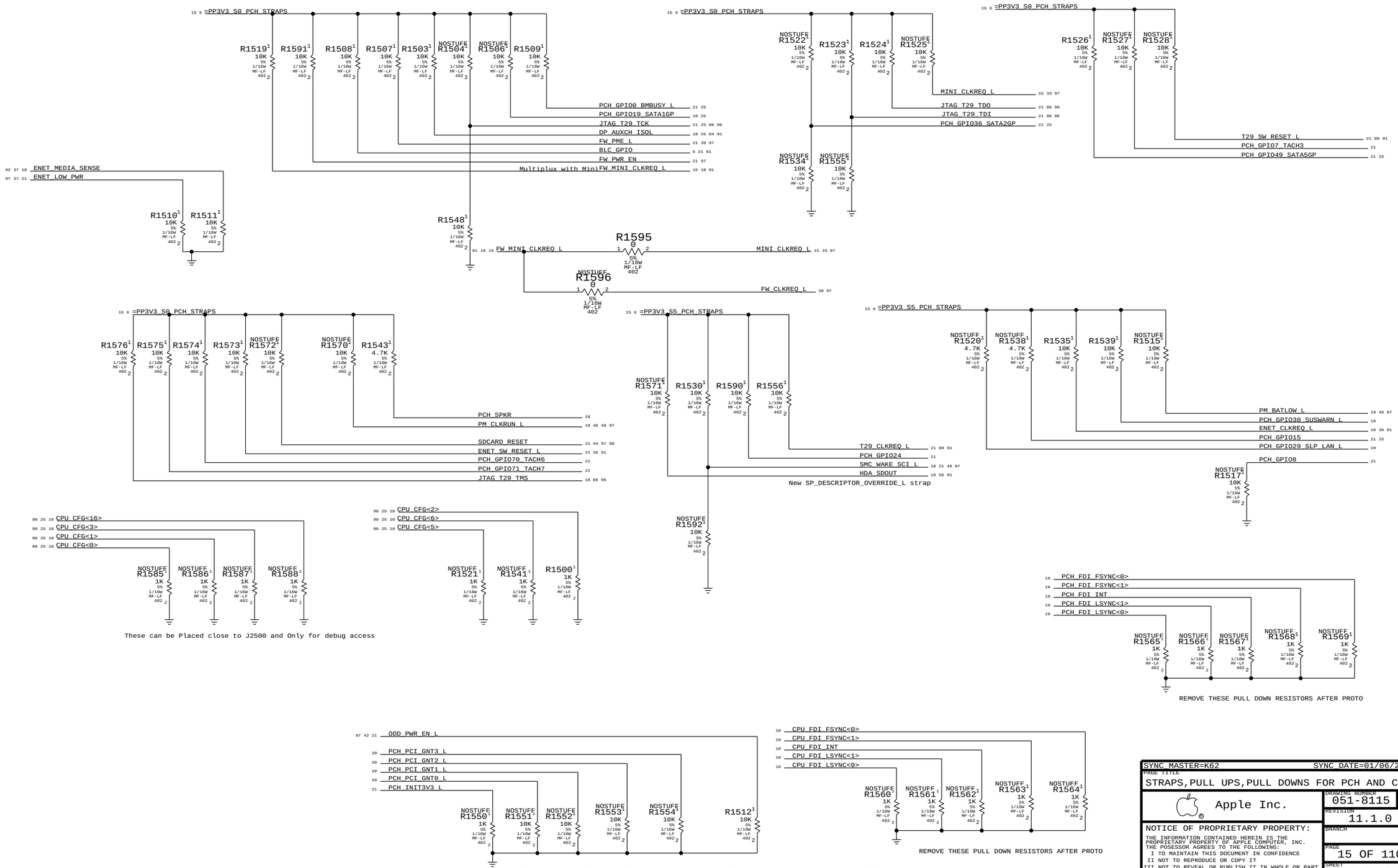

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PAGE TITLE
STRAPS,PULL UPS,PULL DOWNS FOR PCH AND CPU

Apple Inc.

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CPU VCORE DECOUPLING

14x 22UF,0805 INTEL RECOMMENDATION 18X 22UF 0805 (14 Inside cavity and 4 North of processor)

PLACEMENT_NOTE (C1600-C1613):

Place inside socket cavity

16 13 6 65 50 =PPVCORE_S0_CPU

C1600 22UF 20% 6.3V CERM-X5R 805-3
C1601 22UF 20% 6.3V CERM-X5R 805-3
C1602 22UF 20% 6.3V CERM-X5R 805-3
C1603 22UF 20% 6.3V CERM-X5R 805-3
C1604 22UF 20% 6.3V CERM-X5R 805-3
C1605 22UF 20% 6.3V CERM-X5R 805-3
C1606 22UF 20% 6.3V CERM-X5R 805-3
C1607 22UF 20% 6.3V CERM-X5R 805-3
C1608 22UF 20% 6.3V CERM-X5R 805-3
C1609 22UF 20% 6.3V CERM-X5R 805-3

C1610 22UF 20% 6.3V CERM-X5R 805-3
C1611 22UF 20% 6.3V CERM-X5R 805-3
C1612 22UF 20% 6.3V CERM-X5R 805-3
C1613 22UF 20% 6.3V CERM-X5R 805-3

BULK CAPS ON CPU VREG PAGE 72

10x 10UF and 10x 1UF CAPACITORS

Place inside socket cavity

65 50 16 13 6 =PPVCORE_S0_CPU

C1620 10UF 20% 16V X5R 603
C1621 10UF 20% 16V X5R 603
C1622 10UF 20% 16V X5R 603
C1623 10UF 20% 16V X5R 603
C1624 10UF 20% 16V X5R 603
C1625 10UF 20% 16V X5R 603
C1626 10UF 20% 16V X5R 603
C1627 10UF 20% 16V X5R 603
C1628 10UF 20% 16V X5R 603
C1629 10UF 20% 16V X5R 603

C1630 1UF 10% 16V X5R 402
C1631 1UF 10% 16V X5R 402
C1632 1UF 10% 16V X5R 402
C1633 1UF 10% 16V X5R 402
C1634 1UF 10% 16V X5R 402
C1635 1UF 10% 16V X5R 402
C1636 1UF 10% 16V X5R 402
C1637 1UF 10% 16V X5R 402
C1638 1UF 10% 16V X5R 402
C1639 1UF 10% 16V X5R 402

CPU VCCIO DECOUPLING

8X 22UF 0805, 6X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805,16X 0805 placeholders

PLACEMENT_NOTE (C1650-C1657):

Place under socket cavity on secondary side.

13 11 10 6 65 =PPVCCIO_S0_CPU

C1650 22UF 20% 6.3V CERM-X5R 805
C1651 22UF 20% 6.3V CERM-X5R 805
C1652 22UF 20% 6.3V CERM-X5R 805
C1653 22UF 20% 6.3V CERM-X5R 805
C1654 22UF 20% 6.3V CERM-X5R 805
C1655 22UF 20% 6.3V CERM-X5R 805
C1656 22UF 20% 6.3V CERM-X5R 805
C1657 22UF 20% 6.3V CERM-X5R 805

PLACEMENT_NOTE (C1660-C1665):

Place at edge of socket.

BULK CAPS ON CPU VREG PAGE 72

C1660 10uF 20% 6.3V X5R 603
C1661 10uF 20% 6.3V X5R 603
C1662 10uF 20% 6.3V X5R 603
C1663 10uF 20% 6.3V X5R 603
C1664 10uF 20% 6.3V X5R 603
C1665 10uF 20% 6.3V X5R 603

C1670 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

Memory (CPU VCCDDR) DECOUPLING

6x 22uF 0805, 5x 1uF 0402. INTEL RECOMMENDATION 9X 22uF 0805

28 13 11 6 29 =PP1V5_S0_CPU_MEM

C1676 22uF 20% 6.3V CERM-X5R 805
C1677 22uF 20% 6.3V CERM-X5R 805
C1678 22uF 20% 6.3V CERM-X5R 805
C1679 22uF 20% 6.3V CERM-X5R 805
C1680 22uF 20% 6.3V CERM-X5R 805
C1681 22uF 20% 6.3V CERM-X5R 805
C1682 1UF 10% 16V X5R 402
C1683 1UF 10% 16V X5R 402
C1684 1UF 10% 16V X5R 402
C1685 1UF 10% 16V X5R 402
C1686 1UF 10% 16V X5R 402

Note: VCCSA decoupling is on regulator page

PLL (CPU VCCSFR) DECOUPLING

2x 47uF, 1x 22uF 0805, 1x 10uF 0603, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402. INTEL RECOMMENDATION 10x 10uF 0805

13 6 =PP1V8_S0_CPU_PLL

C1693 1UF 10% 16V X5R 402
C1694 1UF 10% 16V X5R 402
C1692 2.2UF 10% 6.3V X5R 402
C1691 4.7UF 10% 6.3V X5R-CERM 603
C1695 10UF 20% 6.3V X5R 603
C1690 22uF 20% 6.3V CERM-X5R 805
C1696 47UF 20% 6.3V X5R 0805
C1697 47UF 20% 6.3V X5R 0805

BULK CAPS ON VTT REG PAGE 78

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PAGE TITLE
CPU NON-GFX DECOUPLING

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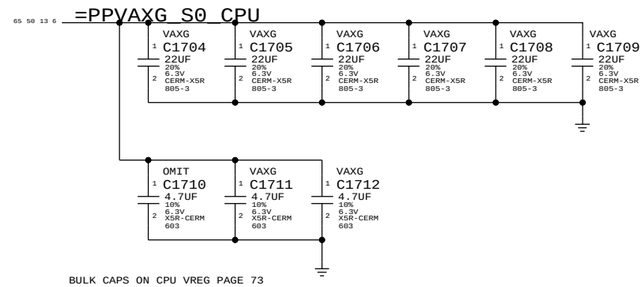
VAXG DECOUPLING

INTEL RECOMMENDATION 6X22UF 0805,3X 4.7UF

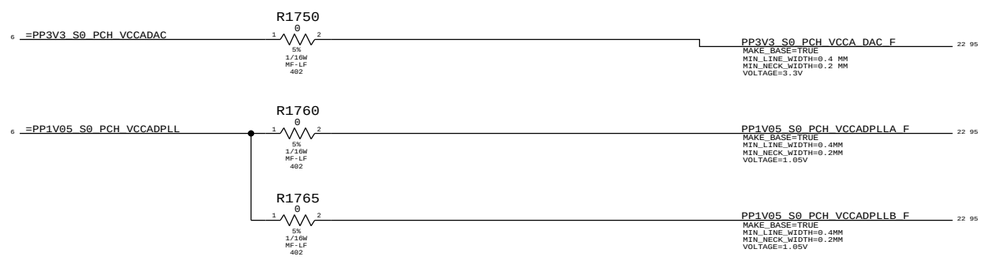
PLACEMENT_NOTE (C1704-C1709):

Place inside socket cavity



BULK CAPS ON CPU VREG PAGE 73

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
138S0586	1	CAP,4.7UF,10%,6.3V,0603	C1710	VAXG
113S0022	1	RES,0 OHM,5%,0603	C1710	NO_VAXG



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PAGE TITLE
GFX DECOUPLING & PCH PWR ALIAS

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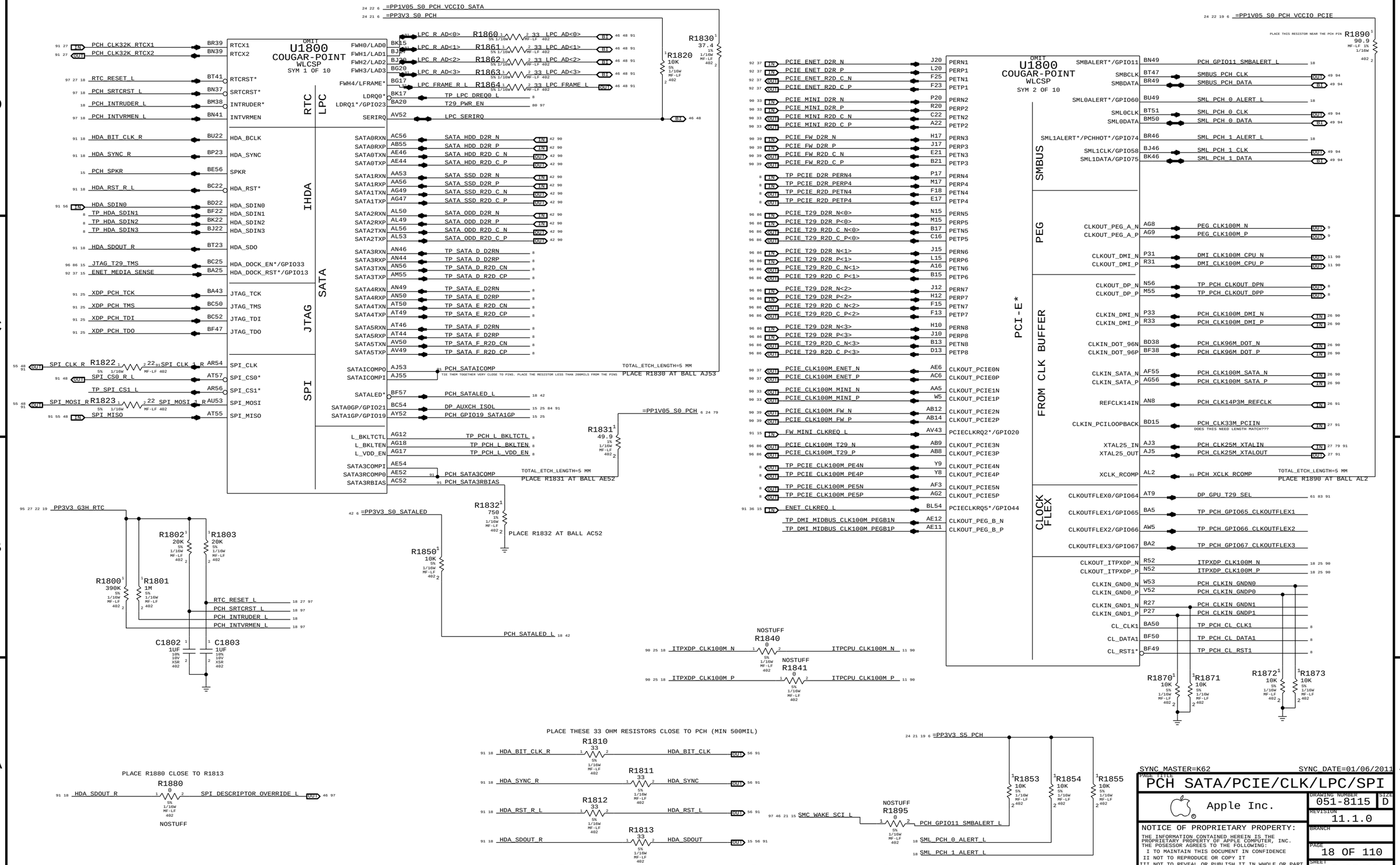

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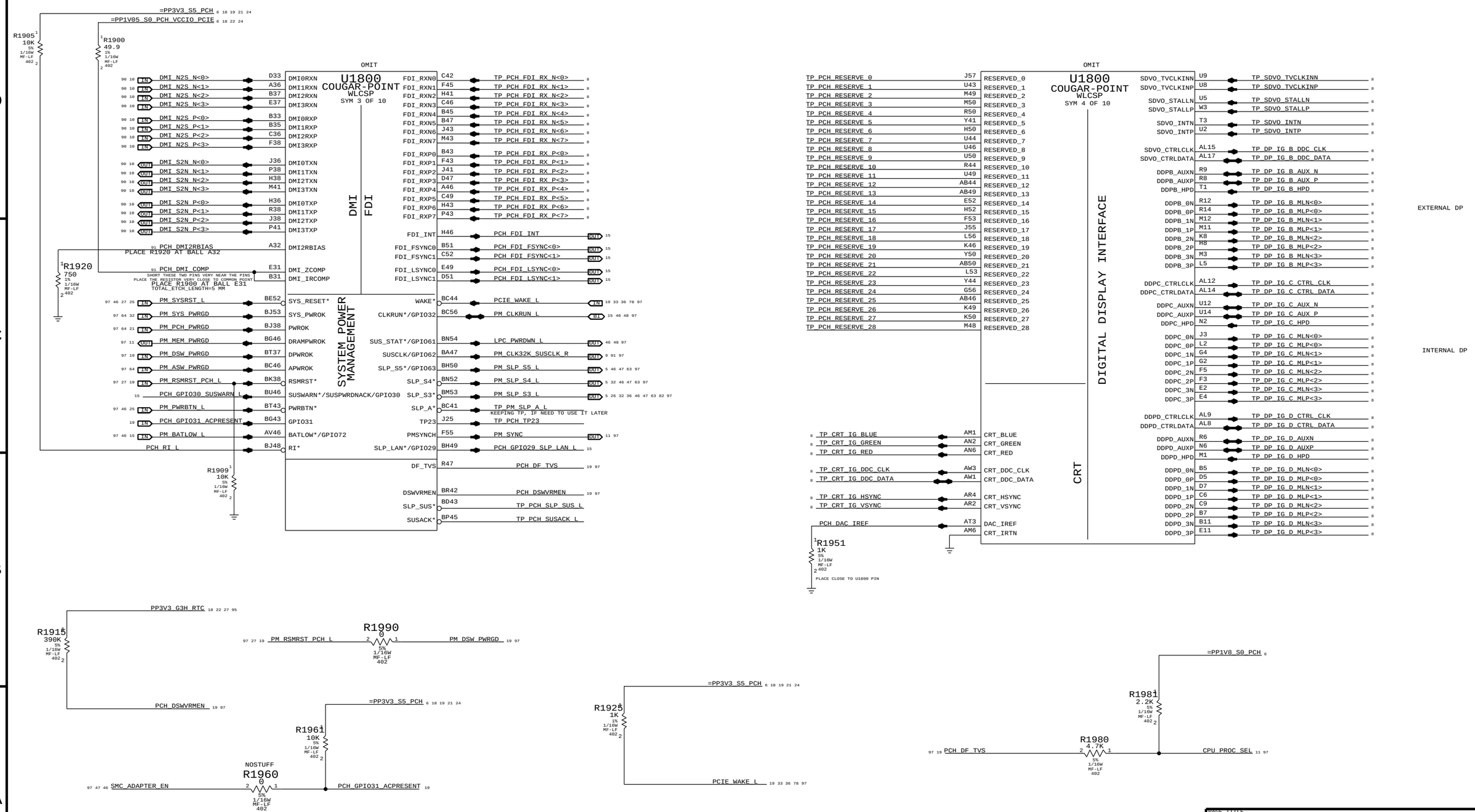

PAGE TITLE
PCH DMI/FDI/GRAPHICS

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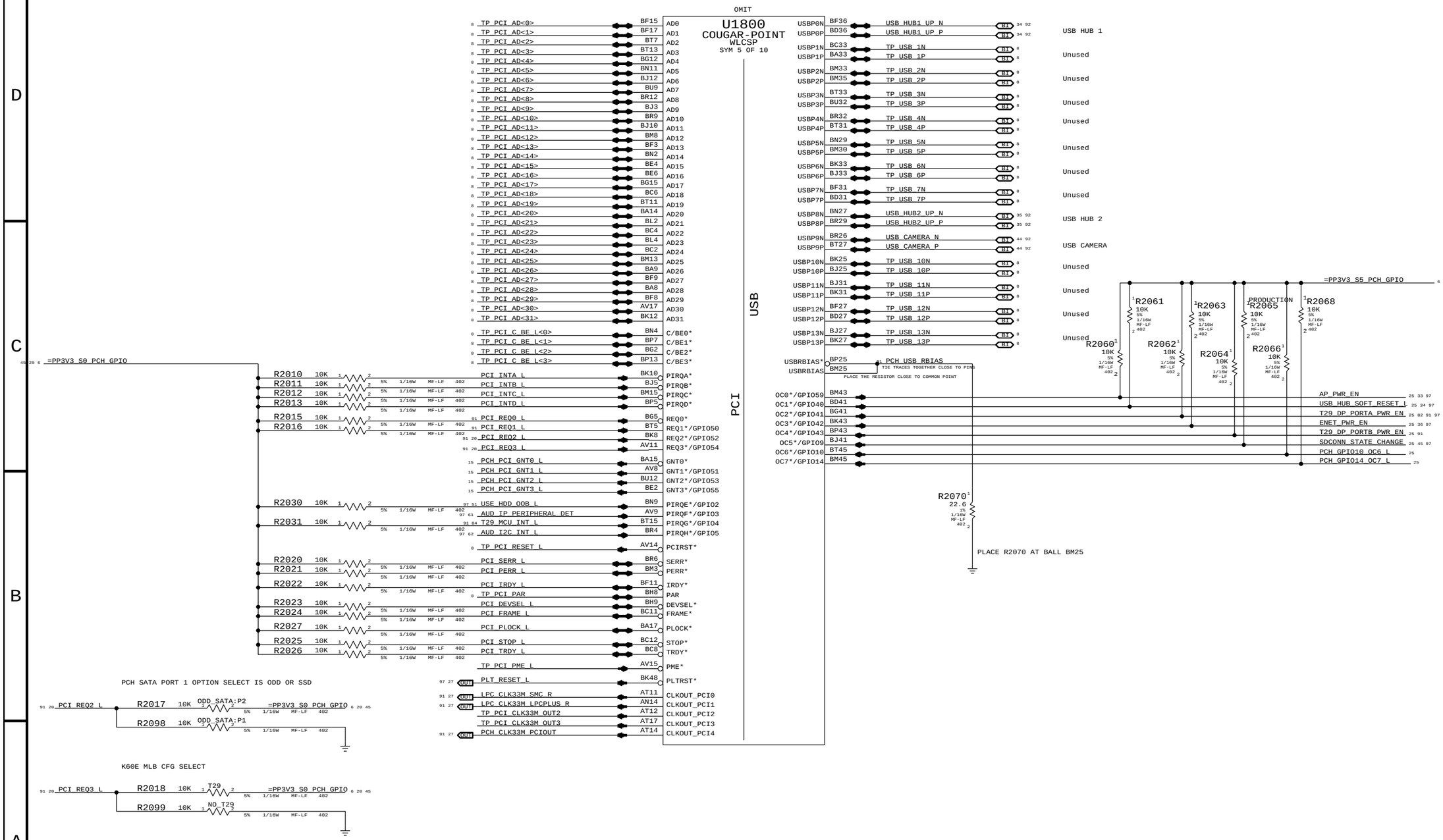

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PAGE TITLE
PCH PCI/FLASHCACHE/USB

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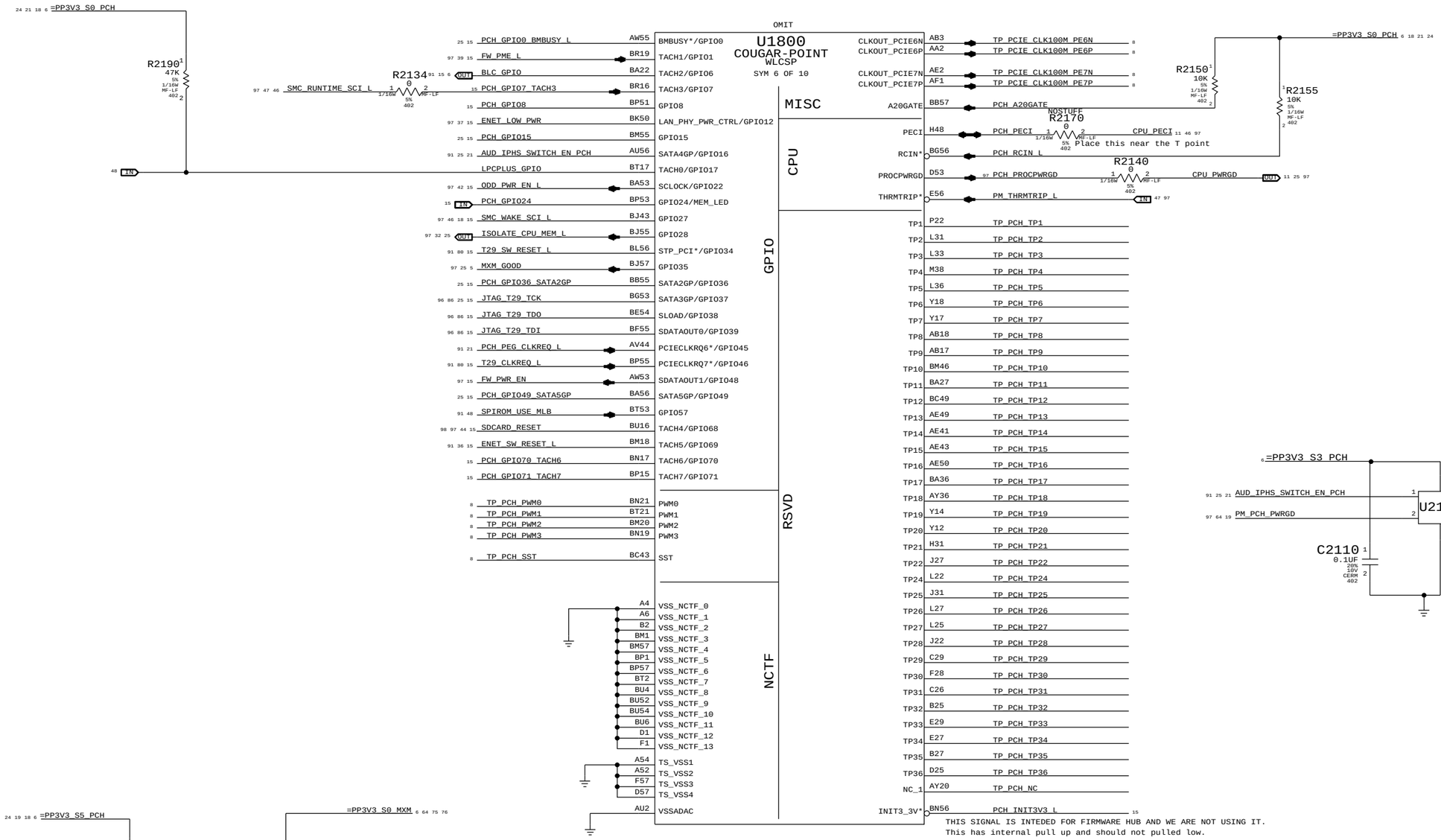

MXM CLKREQ ISOLATION

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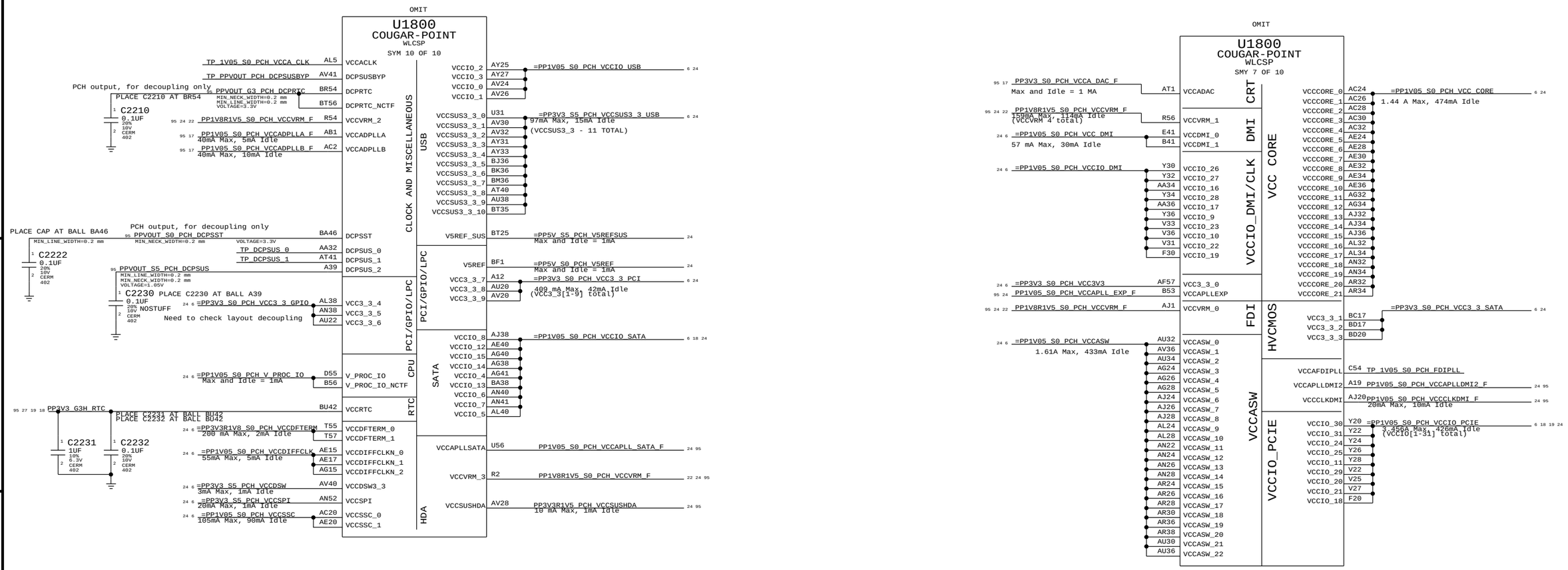

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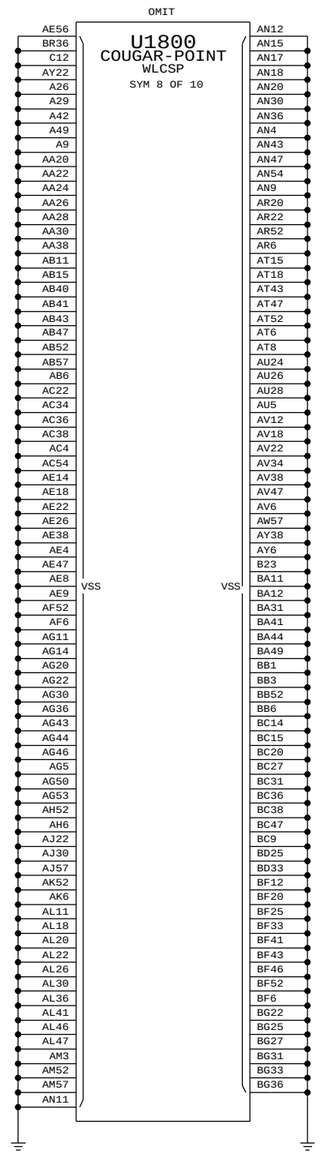

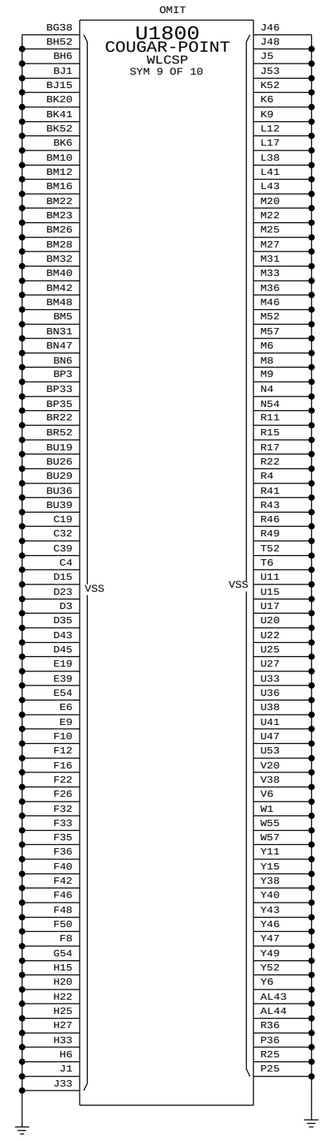

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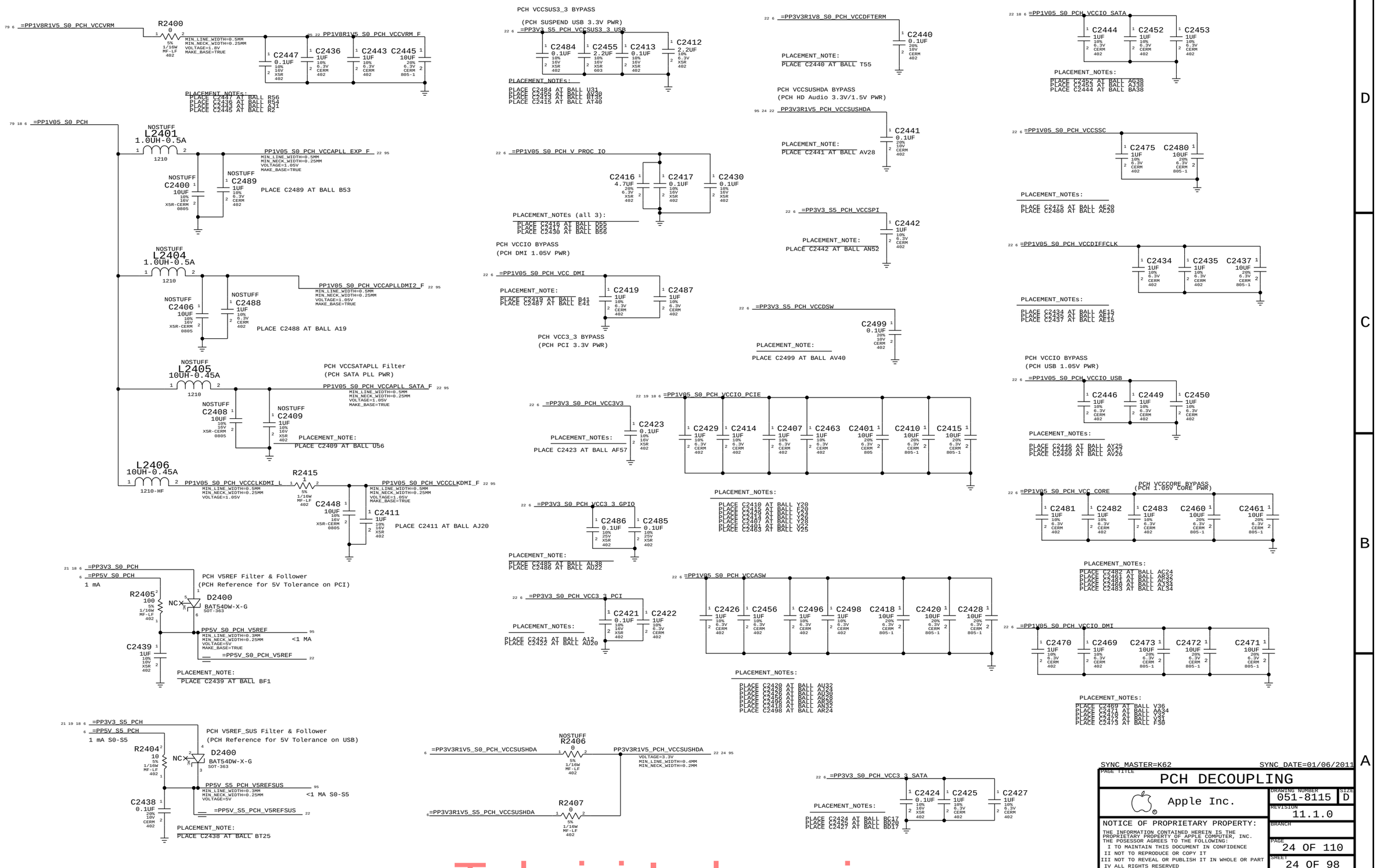

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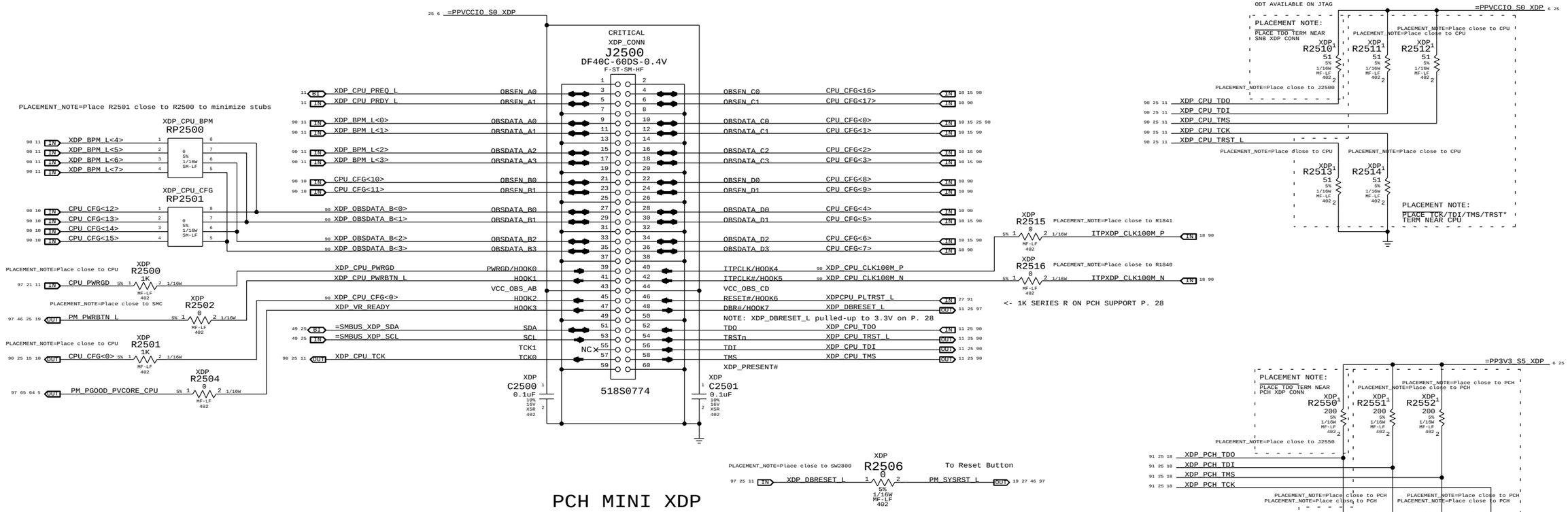
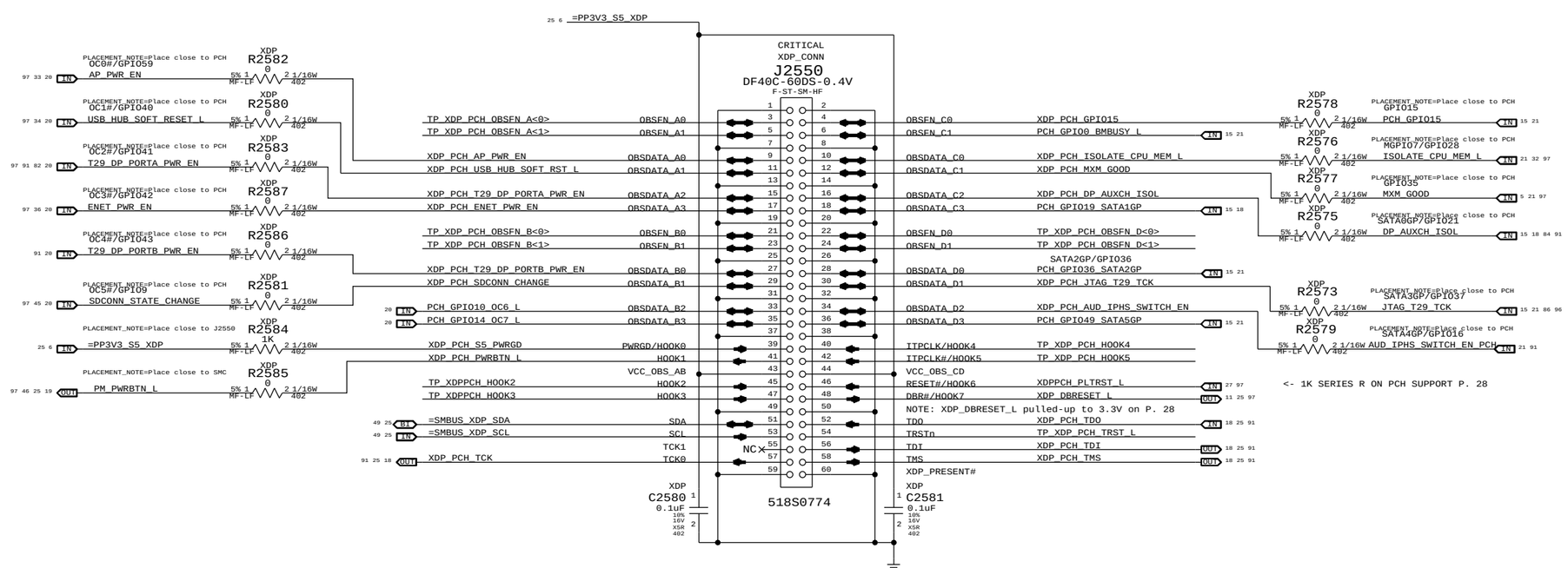
PROCESSOR MINI XDP



PCH MINI XDP



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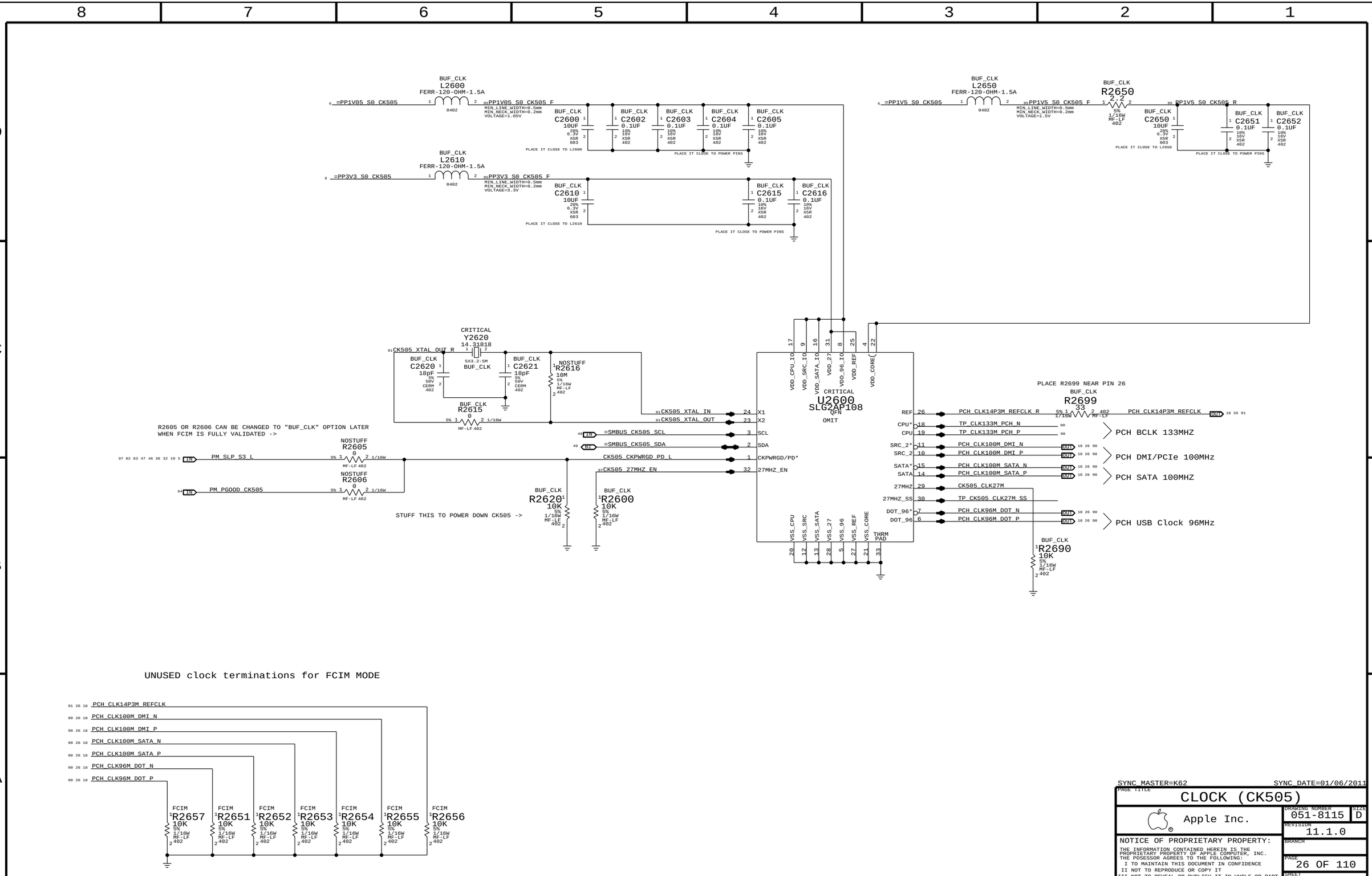

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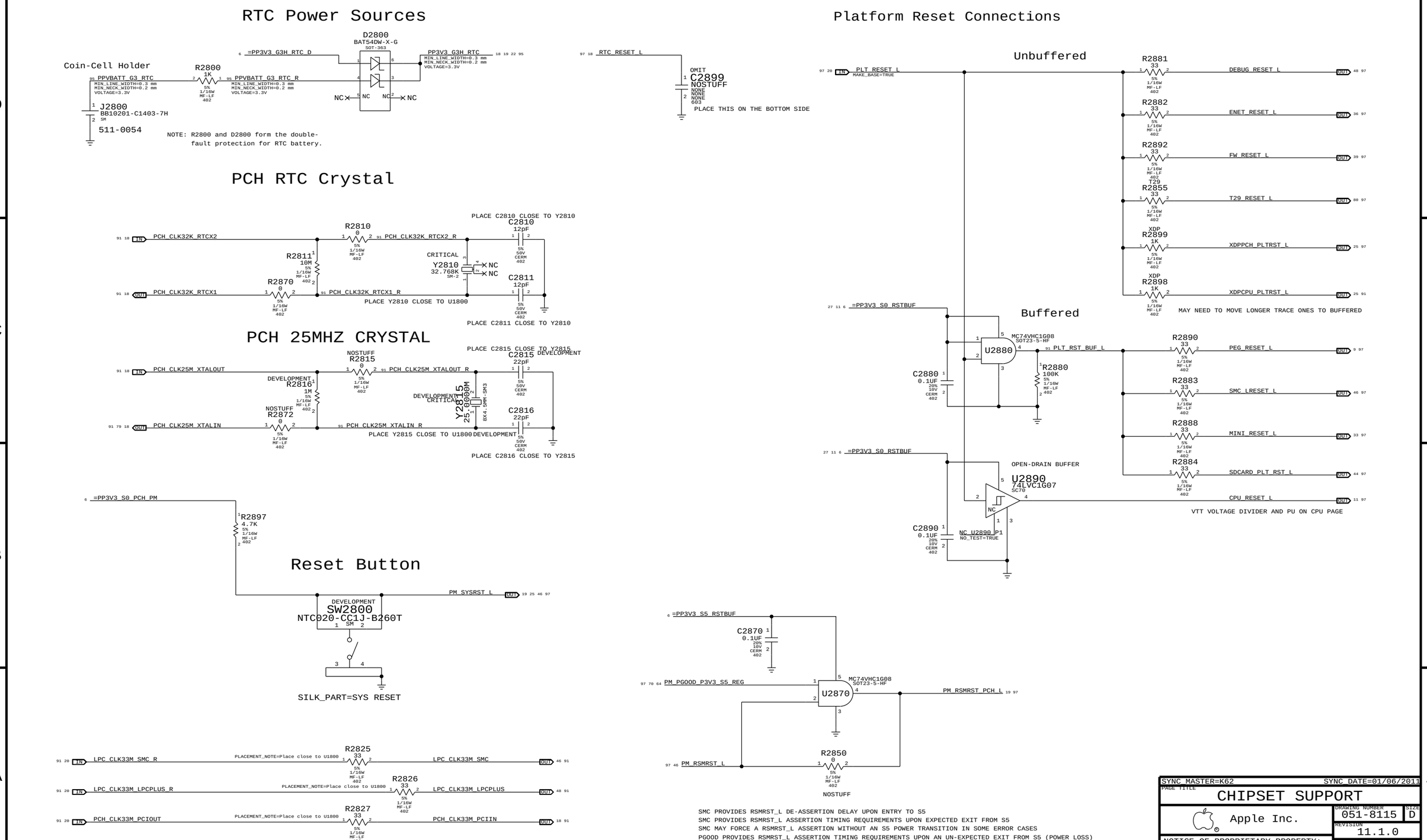

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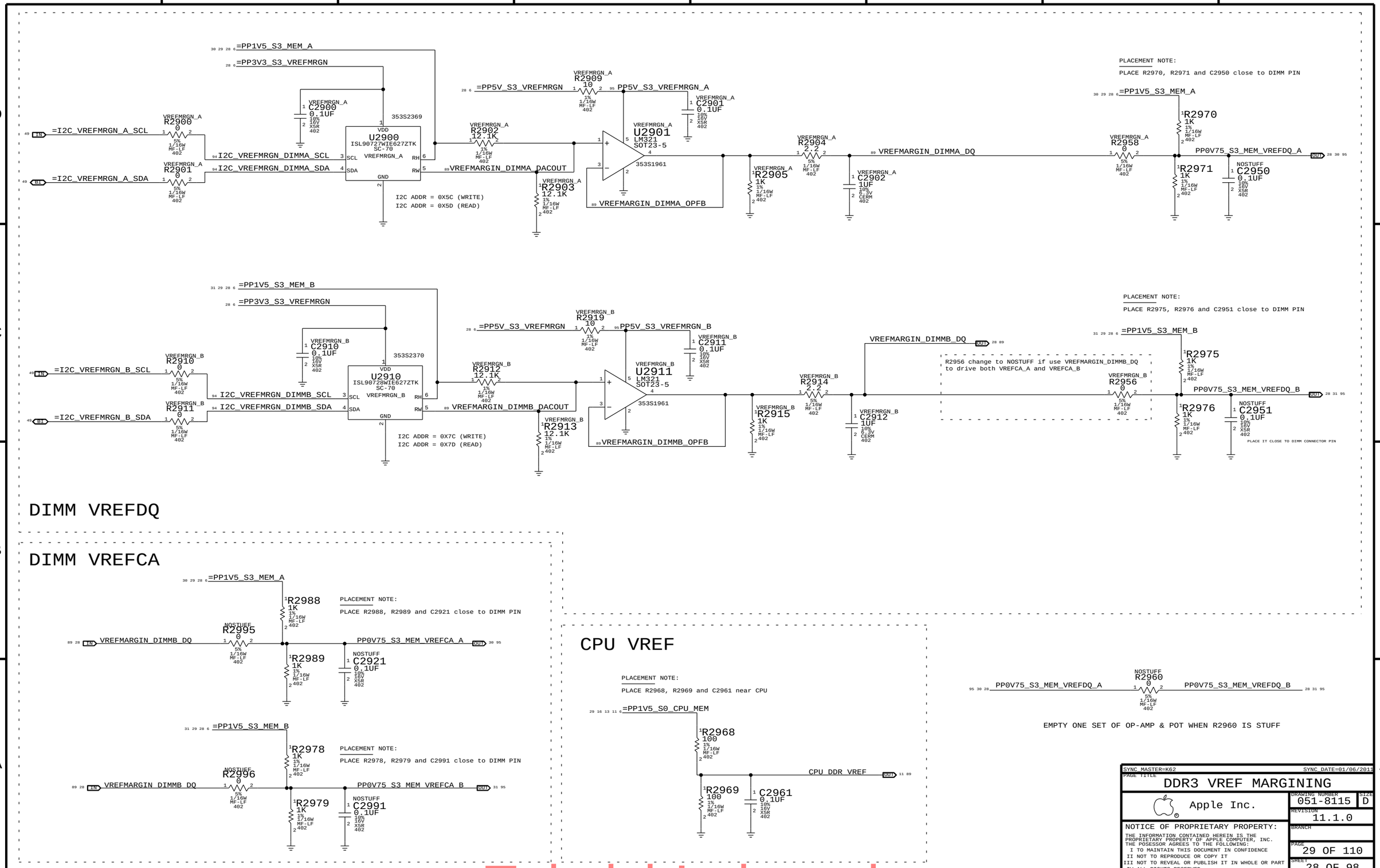

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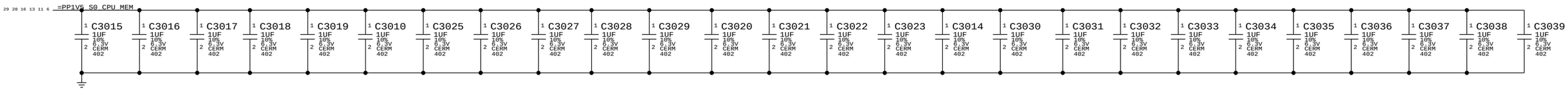
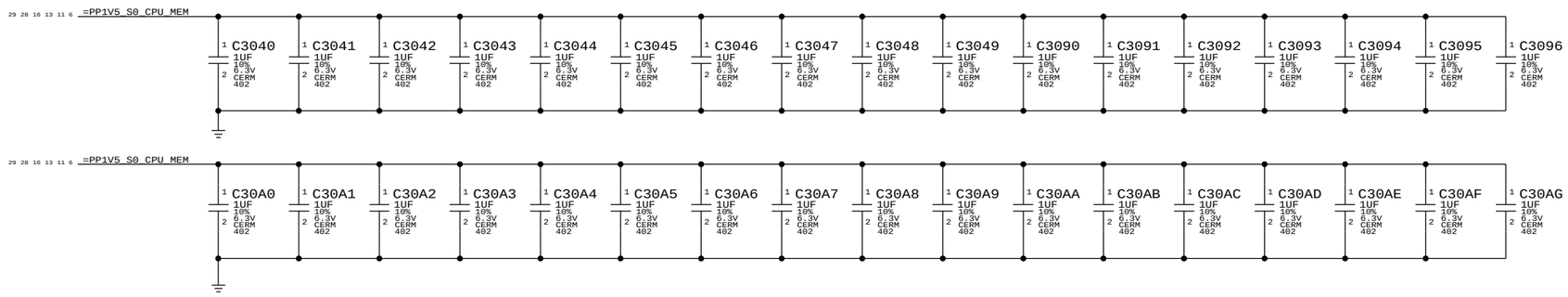
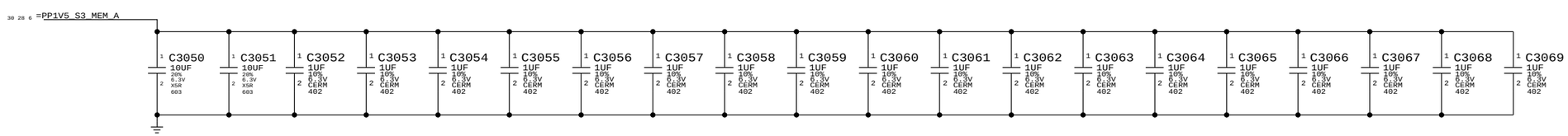
DIMM A (CLOSER TO CPU) CAPS TO STITCH 1V5_CPU_MEM TO GND NEAR DIMM DIMM B (FURTHER FROM CPU)



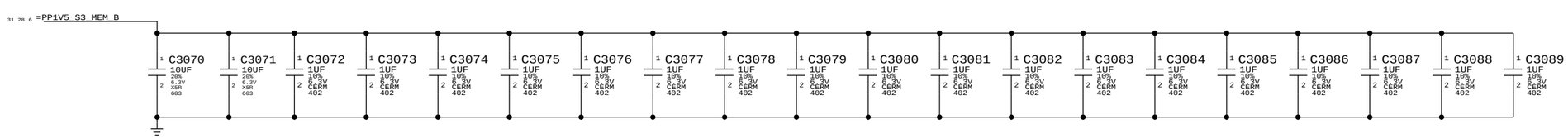
EXTRA DECOUPLING CAPS FOR 1V5_CPU_MEM RAIL



DECOUPLING CAPS FOR 1V5_S3_MEM AT CHANNEL A DIMM CONNECTOR



DECOUPLING CAPS FOR 1V5_S3_MEM AT CHANNEL B DIMM CONNECTOR



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MEMORY CAPS

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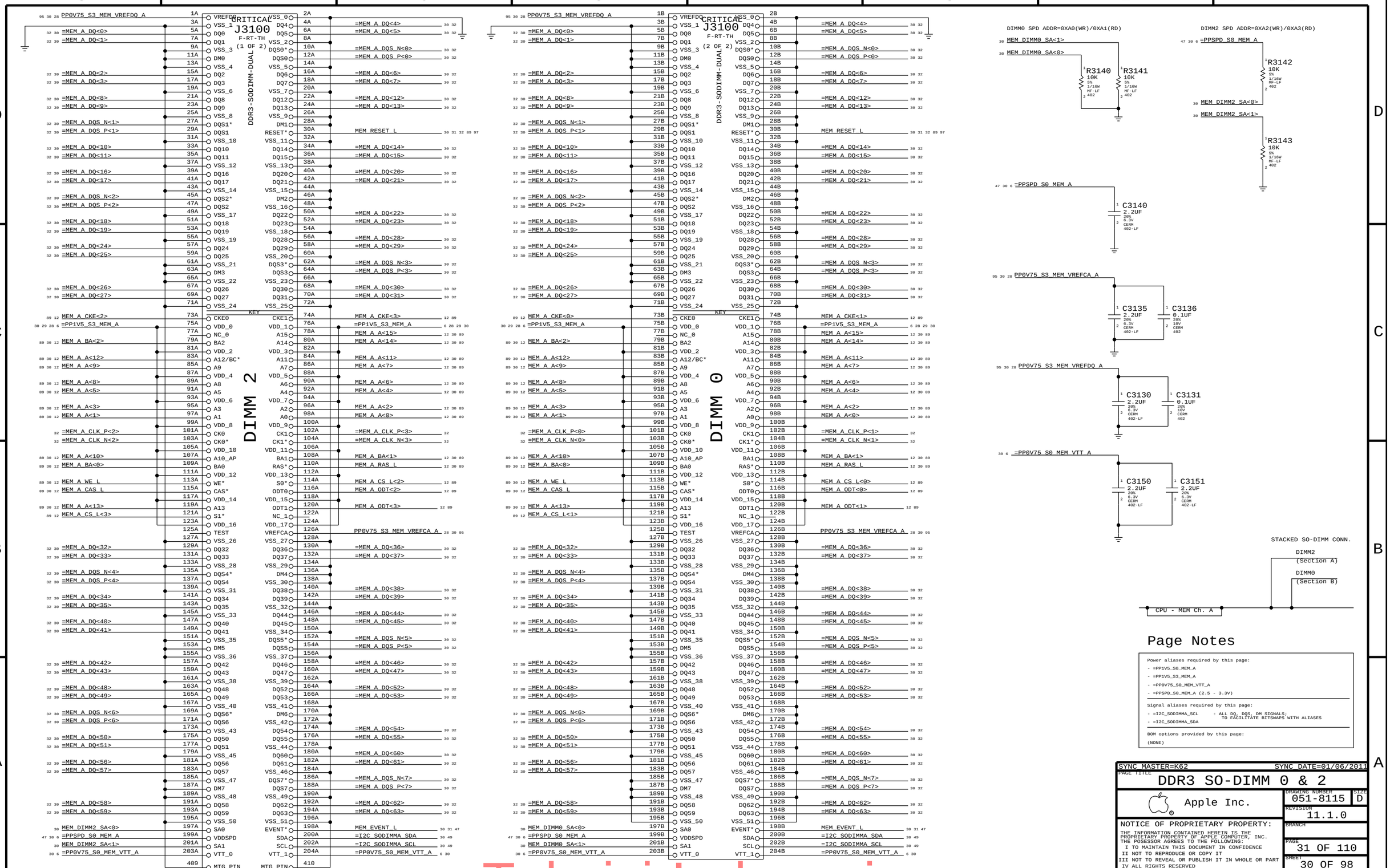

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

- ALL DQ, DQS, DM SIGNALS; TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
(NONE)

SYNC_MASTER=K62	SYNC_DATE=01/06/2011
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Apple Inc.	DRAWING NUMBER: 051-8115 SIZE: D
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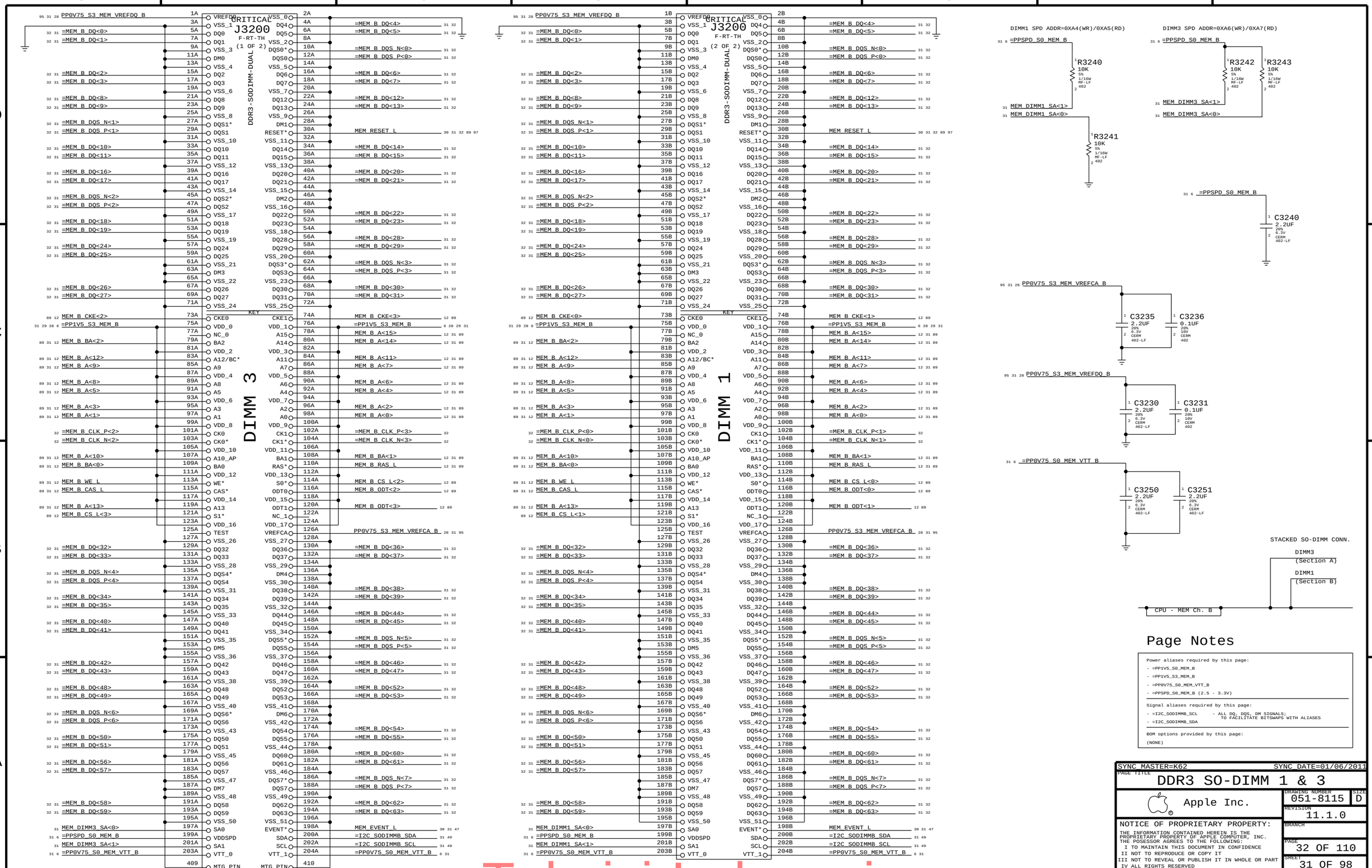

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

- ALL DQ, DQS, DM SIGNALS; TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
(NONE)

SYNC_MASTER=K62	SYNC_DATE=01/06/2011
PAGE TITLE: DDR3 SO-DIMM 1 & 3	
Apple Inc.	DRAWING NUMBER: 051-8115 SIZE: D
	REVISION: 11.1.0
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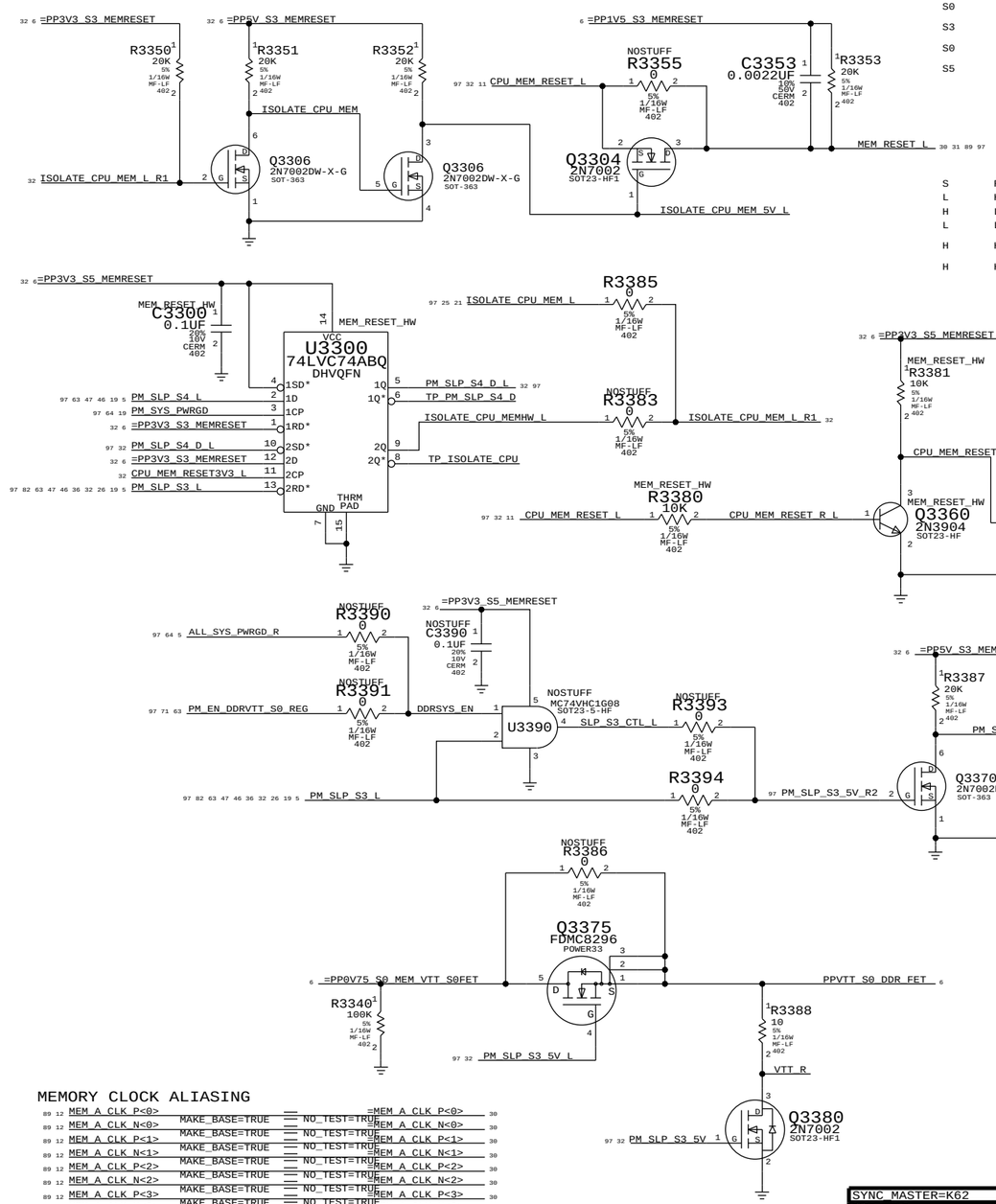
DDR3 RESET SUPPORT

SNB? CANNOT CONTROL THIS SIGNAL DIRECTLY SINCE IT MUST BE HIGH IN SLEEP AND CPU MEM RAILS ARE NOT POWERED IN SLEEP.

	CPU_RESET_L	ISOLATE_L	MEM_RESET_L
S5	0	3.3V	0
S0	0	3.3V	0
S0	1.5V	3.3V	1.5V
S3	0	0	1.5V
S0	1.5V	3.3V	1.5V
S5	0	3.3V	0

S	R	CLK	D	Q	QB
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	POSEDGE	L	L	H
H	H	POSEDGE	H	H	L



CPU CHANNEL A DQS 0 -> DIMM A DQS 7

MEM_A_DQS_N<0>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_N<7>	
MEM_A_DQS_P<0>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_P<7>	
MEM_A_DQ<7>	MAKE_BASE=TRUE		=MEM_A_DQ<57>	
MEM_A_DQ<6>	MAKE_BASE=TRUE		=MEM_A_DQ<56>	
MEM_A_DQ<5>	MAKE_BASE=TRUE		=MEM_A_DQ<58>	
MEM_A_DQ<4>	MAKE_BASE=TRUE		=MEM_A_DQ<59>	
MEM_A_DQ<3>	MAKE_BASE=TRUE		=MEM_A_DQ<60>	
MEM_A_DQ<2>	MAKE_BASE=TRUE		=MEM_A_DQ<61>	
MEM_A_DQ<1>	MAKE_BASE=TRUE		=MEM_A_DQ<62>	
MEM_A_DQ<0>	MAKE_BASE=TRUE		=MEM_A_DQ<63>	

CPU CHANNEL A DQS 1 -> DIMM A DQS 6

MEM_A_DQS_N<1>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_N<6>	
MEM_A_DQS_P<1>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_P<6>	
MEM_A_DQ<15>	MAKE_BASE=TRUE		=MEM_A_DQ<49>	
MEM_A_DQ<14>	MAKE_BASE=TRUE		=MEM_A_DQ<52>	
MEM_A_DQ<13>	MAKE_BASE=TRUE		=MEM_A_DQ<51>	
MEM_A_DQ<12>	MAKE_BASE=TRUE		=MEM_A_DQ<50>	
MEM_A_DQ<11>	MAKE_BASE=TRUE		=MEM_A_DQ<48>	
MEM_A_DQ<10>	MAKE_BASE=TRUE		=MEM_A_DQ<53>	
MEM_A_DQ<9>	MAKE_BASE=TRUE		=MEM_A_DQ<55>	
MEM_A_DQ<8>	MAKE_BASE=TRUE		=MEM_A_DQ<54>	

CPU CHANNEL A DQS 2 -> DIMM A DQS 5

MEM_A_DQS_N<2>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_N<5>	
MEM_A_DQS_P<2>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_P<5>	
MEM_A_DQ<23>	MAKE_BASE=TRUE		=MEM_A_DQ<40>	
MEM_A_DQ<22>	MAKE_BASE=TRUE		=MEM_A_DQ<45>	
MEM_A_DQ<21>	MAKE_BASE=TRUE		=MEM_A_DQ<46>	
MEM_A_DQ<20>	MAKE_BASE=TRUE		=MEM_A_DQ<47>	
MEM_A_DQ<19>	MAKE_BASE=TRUE		=MEM_A_DQ<41>	
MEM_A_DQ<18>	MAKE_BASE=TRUE		=MEM_A_DQ<44>	
MEM_A_DQ<17>	MAKE_BASE=TRUE		=MEM_A_DQ<43>	
MEM_A_DQ<16>	MAKE_BASE=TRUE		=MEM_A_DQ<42>	

CPU CHANNEL A DQS 3 -> DIMM A DQS 4

MEM_A_DQS_N<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_N<4>	
MEM_A_DQS_P<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_P<4>	
MEM_A_DQ<31>	MAKE_BASE=TRUE		=MEM_A_DQ<37>	
MEM_A_DQ<30>	MAKE_BASE=TRUE		=MEM_A_DQ<33>	
MEM_A_DQ<29>	MAKE_BASE=TRUE		=MEM_A_DQ<35>	
MEM_A_DQ<28>	MAKE_BASE=TRUE		=MEM_A_DQ<34>	
MEM_A_DQ<27>	MAKE_BASE=TRUE		=MEM_A_DQ<36>	
MEM_A_DQ<26>	MAKE_BASE=TRUE		=MEM_A_DQ<32>	
MEM_A_DQ<25>	MAKE_BASE=TRUE		=MEM_A_DQ<38>	
MEM_A_DQ<24>	MAKE_BASE=TRUE		=MEM_A_DQ<39>	

CPU CHANNEL A DQS 4 -> DIMM A DQS 3

MEM_A_DQS_N<4>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_N<3>	
MEM_A_DQS_P<4>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_P<3>	
MEM_A_DQ<39>	MAKE_BASE=TRUE		=MEM_A_DQ<28>	
MEM_A_DQ<38>	MAKE_BASE=TRUE		=MEM_A_DQ<29>	
MEM_A_DQ<37>	MAKE_BASE=TRUE		=MEM_A_DQ<27>	
MEM_A_DQ<36>	MAKE_BASE=TRUE		=MEM_A_DQ<31>	
MEM_A_DQ<35>	MAKE_BASE=TRUE		=MEM_A_DQ<25>	
MEM_A_DQ<34>	MAKE_BASE=TRUE		=MEM_A_DQ<24>	
MEM_A_DQ<33>	MAKE_BASE=TRUE		=MEM_A_DQ<26>	
MEM_A_DQ<32>	MAKE_BASE=TRUE		=MEM_A_DQ<30>	

CPU CHANNEL A DQS 5 -> DIMM A DQS 2

MEM_A_DQS_N<5>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_N<2>	
MEM_A_DQS_P<5>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_P<2>	
MEM_A_DQ<47>	MAKE_BASE=TRUE		=MEM_A_DQ<17>	
MEM_A_DQ<46>	MAKE_BASE=TRUE		=MEM_A_DQ<16>	
MEM_A_DQ<45>	MAKE_BASE=TRUE		=MEM_A_DQ<22>	
MEM_A_DQ<44>	MAKE_BASE=TRUE		=MEM_A_DQ<23>	
MEM_A_DQ<43>	MAKE_BASE=TRUE		=MEM_A_DQ<21>	
MEM_A_DQ<42>	MAKE_BASE=TRUE		=MEM_A_DQ<20>	
MEM_A_DQ<41>	MAKE_BASE=TRUE		=MEM_A_DQ<18>	
MEM_A_DQ<40>	MAKE_BASE=TRUE		=MEM_A_DQ<19>	

CPU CHANNEL A DQS 6 -> DIMM A DQS 1

MEM_A_DQS_N<6>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_N<1>	
MEM_A_DQS_P<6>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_P<1>	
MEM_A_DQ<55>	MAKE_BASE=TRUE		=MEM_A_DQ<12>	
MEM_A_DQ<54>	MAKE_BASE=TRUE		=MEM_A_DQ<13>	
MEM_A_DQ<53>	MAKE_BASE=TRUE		=MEM_A_DQ<10>	
MEM_A_DQ<52>	MAKE_BASE=TRUE		=MEM_A_DQ<15>	
MEM_A_DQ<51>	MAKE_BASE=TRUE		=MEM_A_DQ<8>	
MEM_A_DQ<50>	MAKE_BASE=TRUE		=MEM_A_DQ<9>	
MEM_A_DQ<49>	MAKE_BASE=TRUE		=MEM_A_DQ<11>	
MEM_A_DQ<48>	MAKE_BASE=TRUE		=MEM_A_DQ<14>	

CPU CHANNEL A DQS 7 -> DIMM A DQS 0

MEM_A_DQS_N<7>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_N<0>	
MEM_A_DQS_P<7>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_DQS_P<0>	
MEM_A_DQ<63>	MAKE_BASE=TRUE		=MEM_A_DQ<5>	
MEM_A_DQ<62>	MAKE_BASE=TRUE		=MEM_A_DQ<4>	
MEM_A_DQ<61>	MAKE_BASE=TRUE		=MEM_A_DQ<3>	
MEM_A_DQ<60>	MAKE_BASE=TRUE		=MEM_A_DQ<2>	
MEM_A_DQ<59>	MAKE_BASE=TRUE		=MEM_A_DQ<1>	
MEM_A_DQ<58>	MAKE_BASE=TRUE		=MEM_A_DQ<0>	
MEM_A_DQ<57>	MAKE_BASE=TRUE		=MEM_A_DQ<7>	
MEM_A_DQ<56>	MAKE_BASE=TRUE		=MEM_A_DQ<6>	

CPU CHANNEL B DQS 0 -> DIMM B DQS 7

MEM_B_DQS_N<0>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_N<7>	
MEM_B_DQS_P<0>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_P<7>	
MEM_B_DQ<7>	MAKE_BASE=TRUE		=MEM_B_DQ<61>	
MEM_B_DQ<6>	MAKE_BASE=TRUE		=MEM_B_DQ<60>	
MEM_B_DQ<5>	MAKE_BASE=TRUE		=MEM_B_DQ<62>	
MEM_B_DQ<4>	MAKE_BASE=TRUE		=MEM_B_DQ<63>	
MEM_B_DQ<3>	MAKE_BASE=TRUE		=MEM_B_DQ<56>	
MEM_B_DQ<2>	MAKE_BASE=TRUE		=MEM_B_DQ<57>	
MEM_B_DQ<1>	MAKE_BASE=TRUE		=MEM_B_DQ<58>	
MEM_B_DQ<0>	MAKE_BASE=TRUE		=MEM_B_DQ<59>	

CPU CHANNEL B DQS 1 -> DIMM B DQS 6

MEM_B_DQS_N<1>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_N<6>	
MEM_B_DQS_P<1>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_P<6>	
MEM_B_DQ<15>	MAKE_BASE=TRUE		=MEM_B_DQ<51>	
MEM_B_DQ<14>	MAKE_BASE=TRUE		=MEM_B_DQ<54>	
MEM_B_DQ<13>	MAKE_BASE=TRUE		=MEM_B_DQ<53>	
MEM_B_DQ<12>	MAKE_BASE=TRUE		=MEM_B_DQ<52>	
MEM_B_DQ<11>	MAKE_BASE=TRUE		=MEM_B_DQ<48>	
MEM_B_DQ<10>	MAKE_BASE=TRUE		=MEM_B_DQ<49>	
MEM_B_DQ<9>	MAKE_BASE=TRUE		=MEM_B_DQ<50>	
MEM_B_DQ<8>	MAKE_BASE=TRUE		=MEM_B_DQ<55>	

CPU CHANNEL B DQS 2 -> DIMM B DQS 5

MEM_B_DQS_N<2>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_N<5>	
MEM_B_DQS_P<2>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_P<5>	
MEM_B_DQ<23>	MAKE_BASE=TRUE		=MEM_B_DQ<45>	
MEM_B_DQ<22>	MAKE_BASE=TRUE		=MEM_B_DQ<40>	
MEM_B_DQ<21>	MAKE_BASE=TRUE		=MEM_B_DQ<42>	
MEM_B_DQ<20>	MAKE_BASE=TRUE		=MEM_B_DQ<47>	
MEM_B_DQ<19>	MAKE_BASE=TRUE		=MEM_B_DQ<44>	
MEM_B_DQ<18>	MAKE_BASE=TRUE		=MEM_B_DQ<41>	
MEM_B_DQ<17>	MAKE_BASE=TRUE		=MEM_B_DQ<46>	
MEM_B_DQ<16>	MAKE_BASE=TRUE		=MEM_B_DQ<43>	

CPU CHANNEL B DQS 3 -> DIMM B DQS 4

MEM_B_DQS_N<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_N<4>	
MEM_B_DQS_P<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_P<4>	
MEM_B_DQ<31>	MAKE_BASE=TRUE		=MEM_B_DQ<32>	
MEM_B_DQ<30>	MAKE_BASE=TRUE		=MEM_B_DQ<39>	
MEM_B_DQ<29>	MAKE_BASE=TRUE		=MEM_B_DQ<37>	
MEM_B_DQ<28>	MAKE_BASE=TRUE		=MEM_B_DQ<38>	
MEM_B_DQ<27>	MAKE_BASE=TRUE		=MEM_B_DQ<35>	
MEM_B_DQ<26>	MAKE_BASE=TRUE		=MEM_B_DQ<34>	
MEM_B_DQ<25>	MAKE_BASE=TRUE		=MEM_B_DQ<36>	
MEM_B_DQ<24>	MAKE_BASE=TRUE		=MEM_B_DQ<33>	

CPU CHANNEL B DQS 4 -> DIMM B DQS 3

MEM_B_DQS_N<4>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_N<3>	
MEM_B_DQS_P<4>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_P<3>	
MEM_B_DQ<39>	MAKE_BASE=TRUE		=MEM_B_DQ<28>	
MEM_B_DQ<38>	MAKE_BASE=TRUE		=MEM_B_DQ<24>	
MEM_B_DQ<37>	MAKE_BASE=TRUE		=MEM_B_DQ<31>	
MEM_B_DQ<36>	MAKE_BASE=TRUE		=MEM_B_DQ<30>	
MEM_B_DQ<35>	MAKE_BASE=TRUE		=MEM_B_DQ<29>	
MEM_B_DQ<34>	MAKE_BASE=TRUE		=MEM_B_DQ<25>	
MEM_B_DQ<33>	MAKE_BASE=TRUE		=MEM_B_DQ<27>	
MEM_B_DQ<32>	MAKE_BASE=TRUE		=MEM_B_DQ<26>	

CPU CHANNEL B DQS 5 -> DIMM B DQS 2

MEM_B_DQS_N<5>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_N<2>	
MEM_B_DQS_P<5>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_P<2>	
MEM_B_DQ<47>	MAKE_BASE=TRUE		=MEM_B_DQ<18>	
MEM_B_DQ<46>	MAKE_BASE=TRUE		=MEM_B_DQ<20>	
MEM_B_DQ<45>	MAKE_BASE=TRUE		=MEM_B_DQ<23>	
MEM_B_DQ<44>	MAKE_BASE=TRUE		=MEM_B_DQ<22>	
MEM_B_DQ<43>	MAKE_BASE=TRUE		=MEM_B_DQ<19>	
MEM_B_DQ<42>	MAKE_BASE=TRUE		=MEM_B_DQ<21>	
MEM_B_DQ<41>	MAKE_BASE=TRUE		=MEM_B_DQ<17>	
MEM_B_DQ<40>	MAKE_BASE=TRUE		=MEM_B_DQ<16>	

CPU CHANNEL B DQS 6 -> DIMM B DQS 1

MEM_B_DQS_N<6>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_N<1>	
MEM_B_DQS_P<6>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_P<1>	
MEM_B_DQ<55>	MAKE_BASE=TRUE		=MEM_B_DQ<8>	
MEM_B_DQ<54>	MAKE_BASE=TRUE		=MEM_B_DQ<14>	
MEM_B_DQ<53>	MAKE_BASE=TRUE		=MEM_B_DQ<10>	
MEM_B_DQ<52>	MAKE_BASE=TRUE		=MEM_B_DQ<11>	
MEM_B_DQ<51>	MAKE_BASE=TRUE		=MEM_B_DQ<9>	
MEM_B_DQ<50>	MAKE_BASE=TRUE		=MEM_B_DQ<15>	
MEM_B_DQ<49>	MAKE_BASE=TRUE		=MEM_B_DQ<12>	
MEM_B_DQ<48>	MAKE_BASE=TRUE		=MEM_B_DQ<13>	

CPU CHANNEL B DQS 7 -> DIMM B DQS 0

MEM_B_DQS_N<7>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_N<0>	
MEM_B_DQS_P<7>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_DQS_P<0>	
MEM_B_DQ<63>	MAKE_BASE=TRUE		=MEM_B_DQ<2>	
MEM_B_DQ<62>	MAKE_BASE=TRUE		=MEM_B_DQ<1>	
MEM_B_DQ<61>	MAKE_BASE=TRUE		=MEM_B_DQ<3>	
MEM_B_DQ<60>	MAKE_BASE=TRUE		=MEM_B_DQ<7>	
MEM_B_DQ<59>	MAKE_BASE=TRUE		=MEM_B_DQ<4>	
MEM_B_DQ<58>	MAKE_BASE=TRUE		=MEM_B_DQ<5>	
MEM_B_DQ<57>	MAKE_BASE=TRUE		=MEM_B_DQ<6>	
MEM_B_DQ<56>	MAKE_BASE=TRUE		=MEM_B_DQ<0>	

MEMORY CLOCK ALIASING

MEM_A_CLK_P<0>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_CLK_P<0>
MEM_A_CLK_N<0>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_CLK_N<0>
MEM_A_CLK_P<1>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_CLK_P<1>
MEM_A_CLK_N<1>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_CLK_N<1>
MEM_A_CLK_P<2>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_CLK_P<2>
MEM_A_CLK_N<2>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_CLK_N<2>
MEM_A_CLK_P<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_CLK_P<3>
MEM_A_CLK_N<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_A_CLK_N<3>
MEM_B_CLK_P<0>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_CLK_P<0>
MEM_B_CLK_N<0>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_CLK_N<0>
MEM_B_CLK_P<1>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_CLK_P<1>
MEM_B_CLK_N<1>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_CLK_N<1>
MEM_B_CLK_P<2>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_CLK_P<2>
MEM_B_CLK_N<2>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_CLK_N<2>
MEM_B_CLK_P<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_CLK_P<3>
MEM_B_CLK_N<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	=MEM_B_CLK_N<3>

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
DDR3 SUPPORT AND BITSWAPS

Apple Inc.

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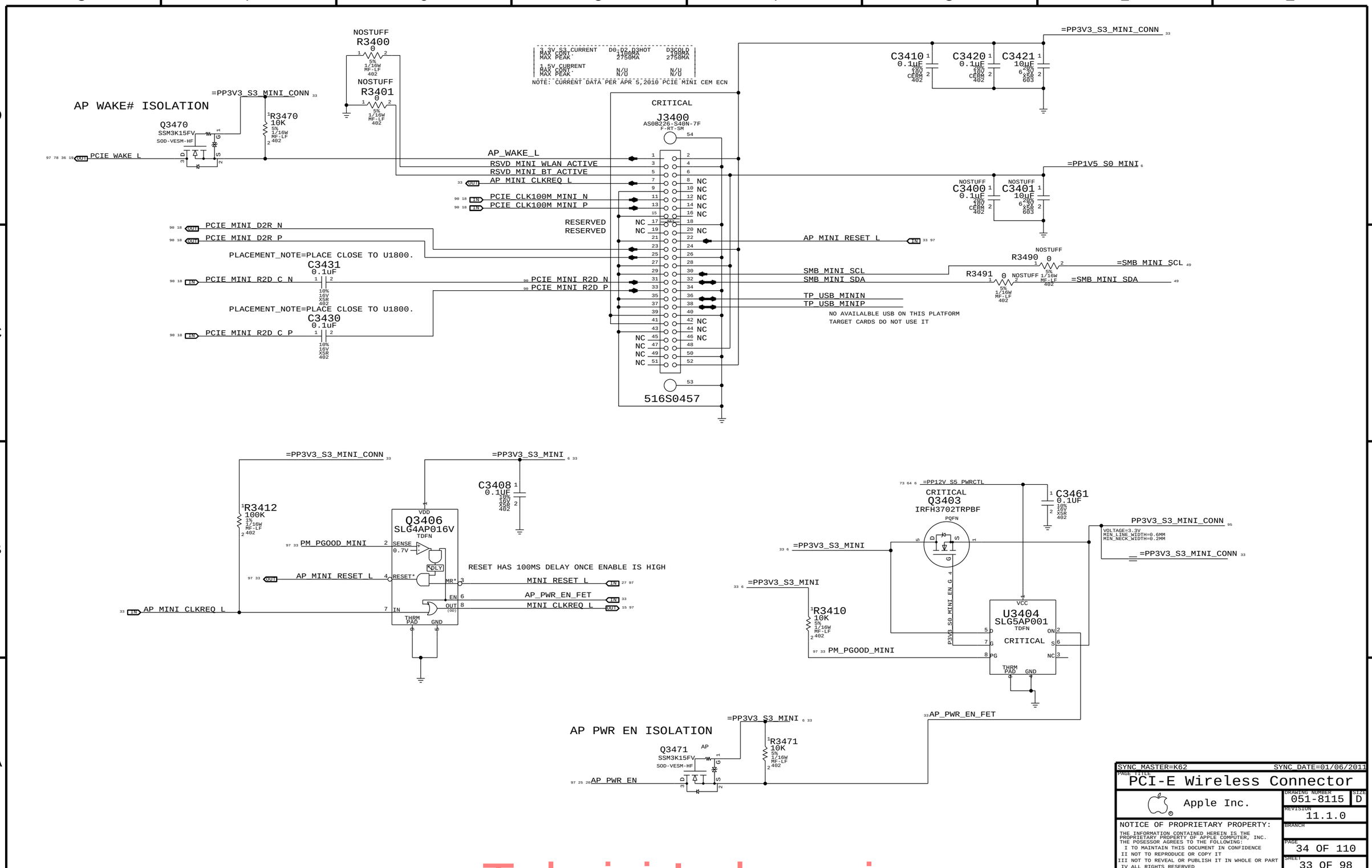

SYNC MASTER=K62	SYNC DATE=01/06/2011
PAGE TITLE	PCI-E Wireless Connector
Apple Inc.	DRAWING NUMBER 051-8115 SIZE D
	REVISION 11.1.0
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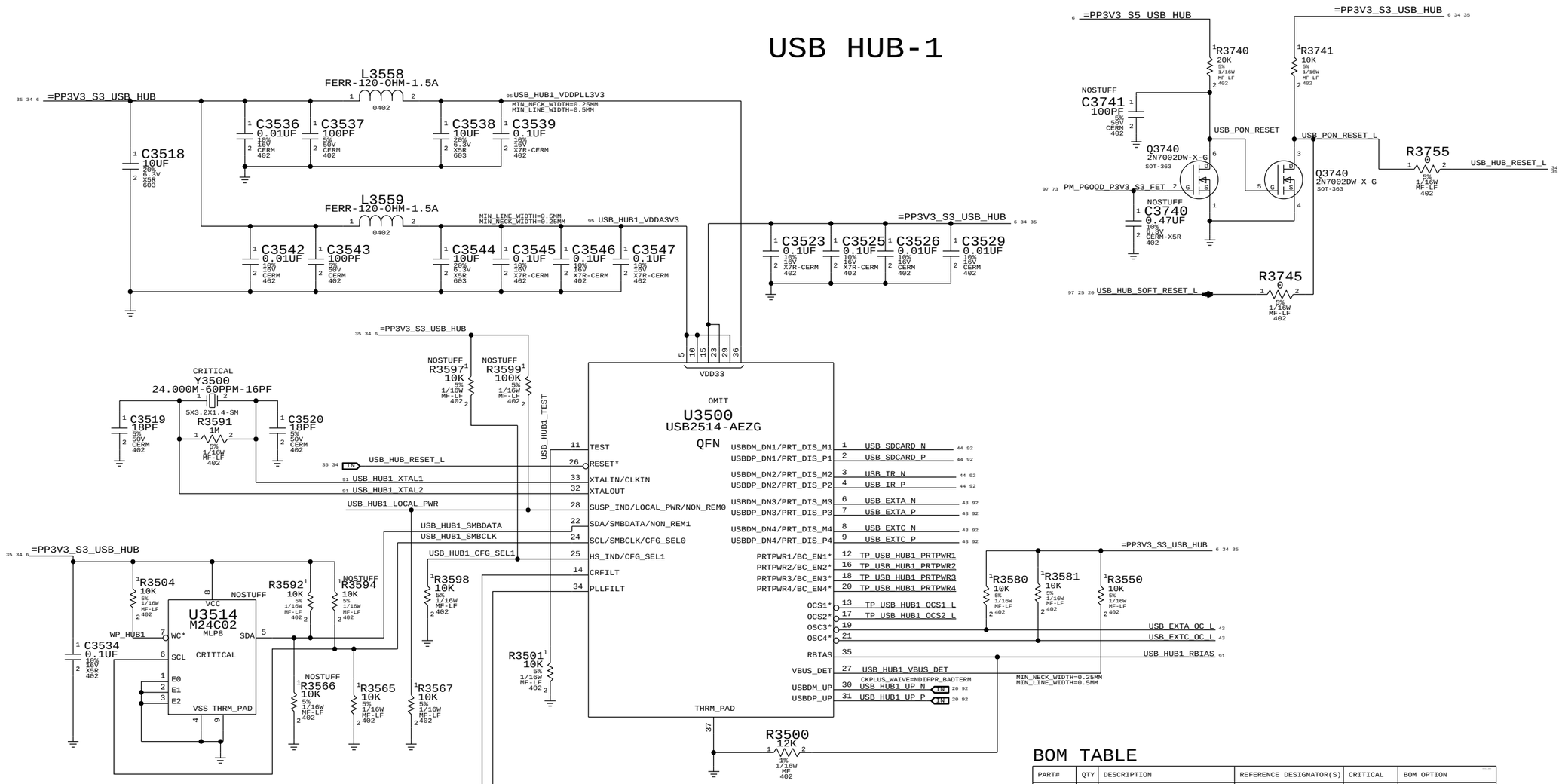
USB HUB-1



	SEL1	SEL0	DESCRIPTION
DEFAULT K23F ==>	0	0	Internal Default with Self powered Operation
	0	1	SMBUS Slave Config
	1	0	Internal Default with Bus powered Operation
	1	1	EEPROM Supported

	NON_REM1	NON_REM0	DESCRIPTION
	0	0	All ports are Non removable
	0	1	Port1 is non removable
DEFAULT K23F ==>	1	0	Port 1 and 2 are non removable
	1	1	Port1,2 and 3 are non Removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0721	2	SMSC USX2061-AEZG	U3500,U3600	CRITICAL	HUB_USX2061
338S0824	2	SMSC USB2514B	U3500,U3600	CRITICAL	HUB_USB2514B

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PAGE TITLE
USB HUB 1

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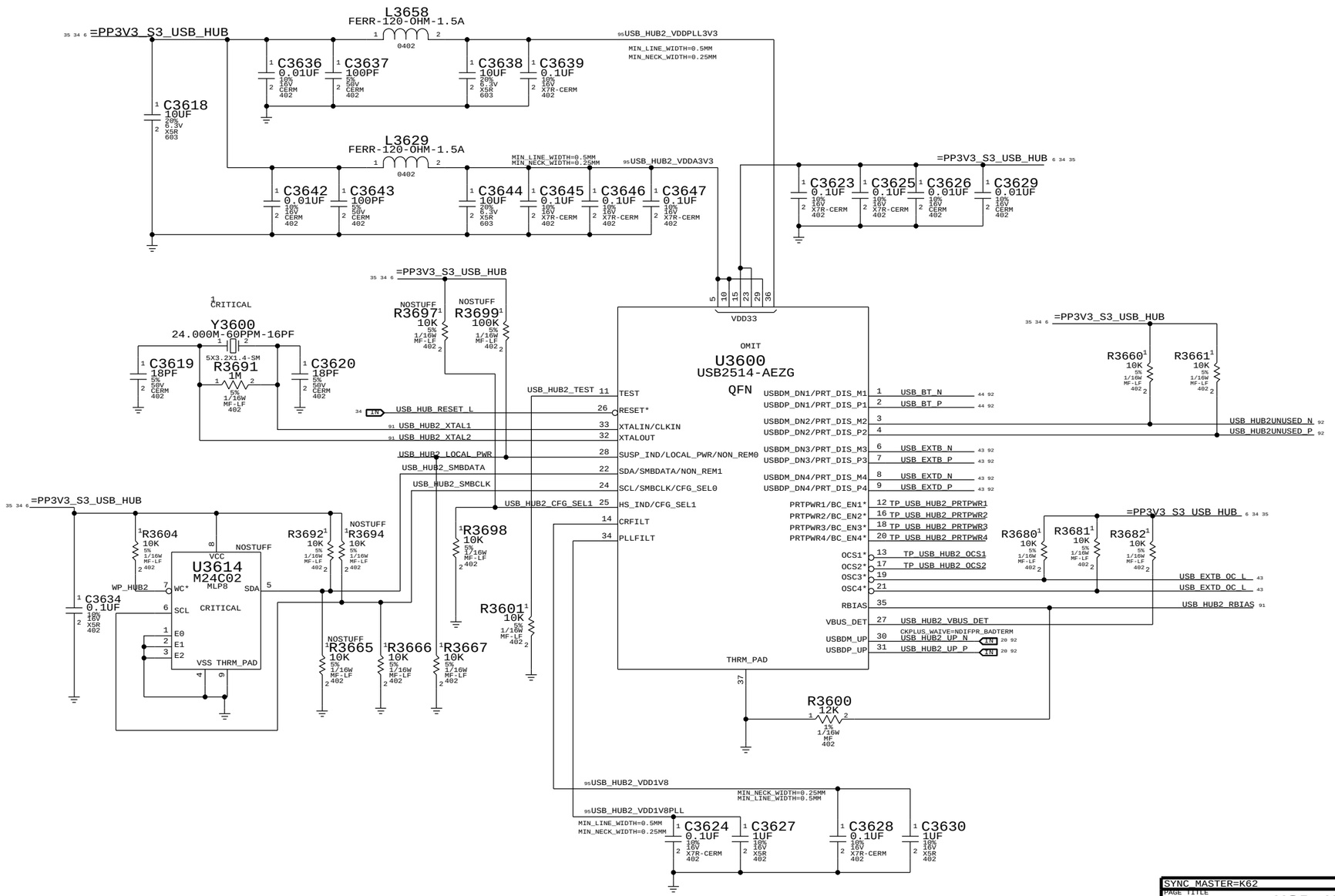
USB HUB-2



SYNC MASTER=K62 SYNC DATE=01/06/2011

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USB HUB 2

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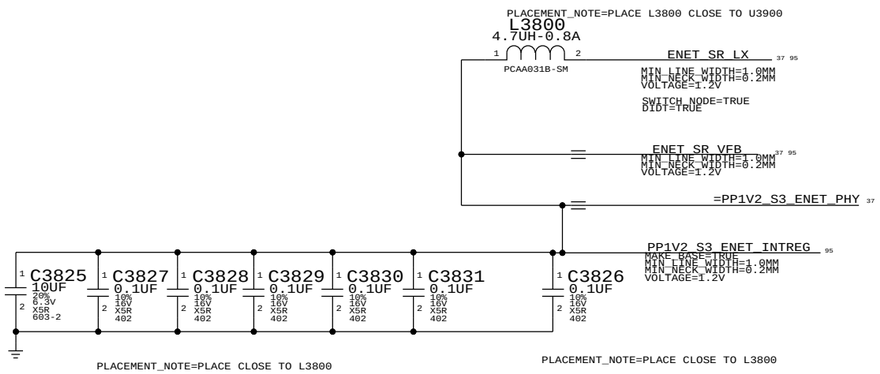
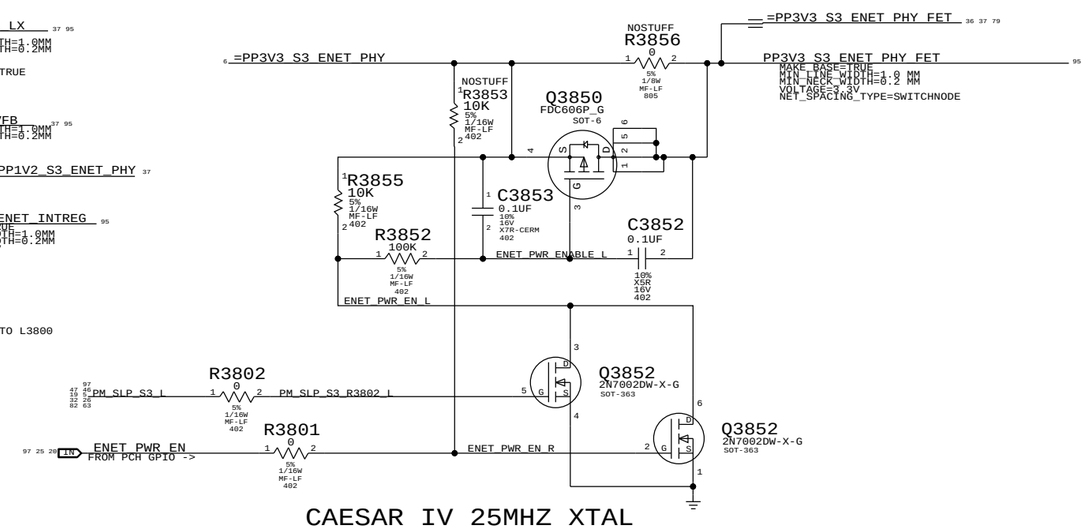
CAESAR IV 1.2V INT.VR CMPTS

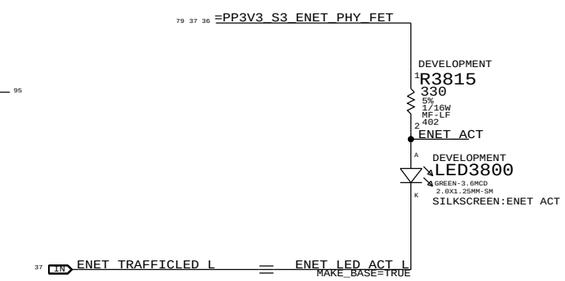


CAESAR IV POWER ENABLE CIRCUIT

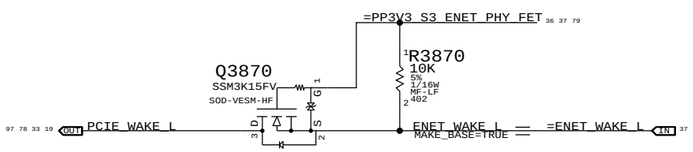
3V3_ENET_PHY_FET = S0 || (S3 POWER && ENET_PWR_EN)



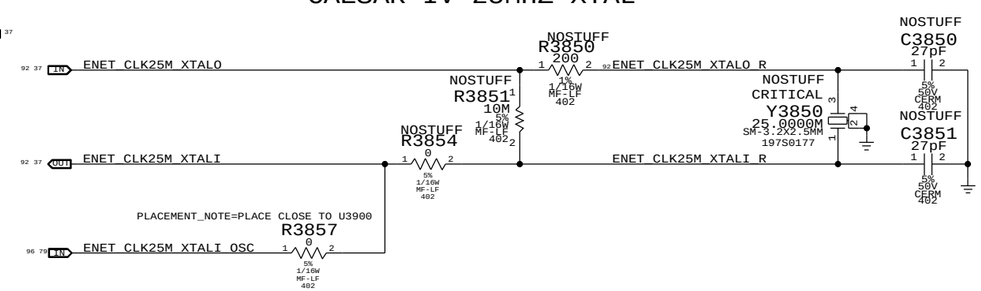
CAESAR IV ACTIVITY LED



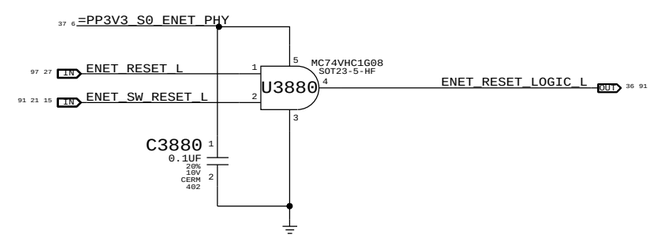
CAESAR IV WAKE# ISOLATION



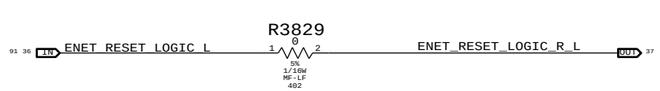
CAESAR IV 25MHZ XTAL



CAESAR IV SW RESET GATING

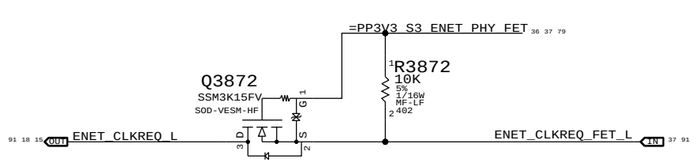


CAESAR IV RESET CONNECTION



CAESAR IV STRAPS (NONE)

CAESAR IV CLKREQ ISOLATION



SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
CAESAR IV SUPPORT

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DRAWING NUMBER 051-8115 SIZE D

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

281mA (1000base-T max power, Caesar IV)

=PP3V3_S3_ENET_PHY_FET

R3901 0 5% 1/16W MF-LF 402 — ENET_3V3_S3_SR_IN (SWITCH_NODE=TRUE, DIDT=TRUE, NET_SPACING_TYPE=SWITCHNODE, MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V)

C3979 4.7UF 20% 6.3V CERM 603

C3980 0.1UF 10% 16V X5R 402

C3981 0.1UF 10% 16V X5R 402

VDD for Card Reader I/O
=PP3V3R1V8_ENET_LR_OUT

CRITICAL L3900 FERR-600-OHM-0.5A SM — PP3V3_S3_ENET_PHY_XTALVDDH (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

R3900 0 5% 1/16W MF-LF 402 — ENET_XTALVDDH (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

C3900 0.1UF 10% 16V X7R-CERM 402

CRITICAL L3905 FERR-600-OHM-0.5A SM — PP3V3_S3_ENET_PHY_BIASVDDH (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

C3905 0.1UF 10% 16V X7R-CERM 402

CRITICAL L3910 FERR-600-OHM-0.5A SM — PP3V3_S3_ENET_PHY_AVDDH (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

R3910 4.7K 5% 1/16W MF-LF 402

C3910 0.1UF 10% 16V X7R-CERM 402

C3911 0.1UF 10% 16V X7R-CERM 402

R3940 4.7K 5% 1/16W MF-LF 402

R3941 4.7K 5% 1/16W MF-LF 402

C3917 0.1UF 10% 16V X7R-CERM 402

C3918 0.1UF 10% 16V X7R-CERM 402

C3915 4.7UF 10% 6.3V X5R-CERM 603

C3916 0.1UF 10% 16V X7R-CERM 402

=PP3V3_S0_ENET_PHY

R3942 1K 5% 1/16W MF-LF 402 — Current Limiting Resistor

C3950 0.1uF 10% 16V X5R 402 — PCIE_ENET_D2R_N

C3951 0.1uF 10% 16V X5R 402 — PCIE_ENET_D2R_P

C3955 0.1uF 10% 16V X5R 402 — PCIE_ENET_R2D_C_P

C3956 0.1uF 10% 16V X5R 402 — PCIE_ENET_R2D_C_N

R3943 0 5% 1/16W MF-LF 402 — =ENET_WAKE_L (See note)

WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

ENET_SR_LX
ENET_SR_VFB

Internal 1.2V Switching Regulator pins.

=PP1V2_S3_ENET_PHY
396mA (1000base-T, Caesar II)

CRITICAL L3920 FERR-600-OHM-0.5A SM — PP1V2_S3_ENET_PHY_AVDDL (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.2V)

C3921 0.1UF 10% 16V X7R-CERM 402

C3920 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL L3925 FERR-600-OHM-0.5A SM — PP1V2_S3_ENET_PHY_PCIEPLL (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.2V)

C3926 0.1UF 10% 16V X7R-CERM 402

C3925 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL L3930 FERR-600-OHM-0.5A SM — PP1V2_S3_ENET_PHY_GPHYPLL (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.2V)

C3931 0.1UF 10% 16V X7R-CERM 402

C3930 4.7UF 10% 6.3V X5R-CERM 603

C3936 0.1UF 10% 16V X7R-CERM 402

C3935 10UF 10% 6.3V X5R 805

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O. Connect only to U3900 pin 20.

=PP3V3R1V8_ENET_LR_OUT

PP3V3R1V8_ENET_LR_OUT_REG (MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.8V)

DEVELOPMENT C3970 4.7UF 10% 6.3V X5R-CERM 603

DEVELOPMENT C3971 0.1UF 10% 16V X7R-CERM 402

C3972 0.1UF 10% 16V X7R-CERM 402 DEVELOPMENT

NOSTUFF R3959 150 5% 1/16W MF-LF 402

NOSTUFF C3959 10PF 5% 50V CERM 402

MUST DO: REMOVE C/R3959 AFTER PROTO 2

OMIT
U3900
BCM57765
QFN-8X8

Pin	Signal	Net
42, 48	AVDDH	
37	BIASVDDH	
17	XTALVDDH	
7	VDDO	
20, 56, 62		
14	SR_VDD	
15	SR_VDDP	
16	SR_LX	
13	SR_VFB	
39, 45, 51	AVDDL	
29	PCIE_PLLVDDL	
32	GPHY_PLLVDDL	
36		
35, 61	VDDC	
58	VMAIN_PRSNT (IPD-ENET)	ENET_VMAIN_PRSNT
27	PCIE_TXD_N	PCIE_ENET_D2R_C_N
28	PCIE_TXD_P	PCIE_ENET_D2R_C_P
33	PCIE_RXD_P	PCIE_ENET_R2D_P
34	PCIE_RXD_N	PCIE_ENET_R2D_N
31	PCIE_REFCLK_P	PCIE_CLK100M_ENET_P
30	PCIE_REFCLK_N	PCIE_CLK100M_ENET_N
11	PERST* (IPD)	ENET_RESET_LOGIC_R_L
12	CLKREQ* (OD)	ENET_CLKREQ_FET_L
3	WAKE* (OD)	ENET_WAKE_R_L
4	LOW_PWR (IPD)	ENET_LOW_PWR
6	SMB_CLK	ENET_SMB_CLK
10	SMD_DATA (IPD-ENETM)	ENET_SMB_DATA
66	SCLK	ENET_SCLK
64	SI/LINKLED*	ENET_MISO
65	SO	ENET_MOSI
63	CS*	ENET_CS_L
2	SPD100LED*/SERIAL_DO (OD)	TP_ENET_SPD100LED_L
67	TRAFFICLED*/SERIAL_DI (OD)	ENET_TRAFFICLED_L
18	XTALI	ENET_CLK25M_XTALI
19	XTALO	ENET_CLK25M_XTALO
38	RDAC	ENET_RDAC
69	THRM_PAD (NO IPU OR IPD-ENET)	
40	TRD0_P	ENETCONN_MDI_P<0>
41	TRD0_N	ENETCONN_MDI_N<0>
44	TRD1_P	ENETCONN_MDI_P<1>
43	TRD1_N	ENETCONN_MDI_N<1>
46	TRD2_P	ENETCONN_MDI_P<2>
47	TRD2_N	ENETCONN_MDI_N<2>
50	TRD3_P	ENETCONN_MDI_P<3>
49	TRD3_N	ENETCONN_MDI_N<3>
5	GPIO_0 (IPD)	NC
8	GPIO_1/CR_BUS_PWR (IPD)	
9	RE*/GPIO_2 (IPD)	ENET_MEDIA_SENSE
1	SD_DETECT/WE* (IPx-ENET)	ENET_SD_DETECT_L
26	CR_CMD/CLE (IPU-ENET)	ENET_SD_CMD
21	CR_CLK/RY_BY*	ENET_SD_CLK
25	CR_DATA0 (IPU-ENET)	ENET_CR_DATA<0>
24	CR_DATA1	ENET_CR_DATA<1>
23	CR_DATA2	ENET_CR_DATA<2>
22	CR_DATA3	ENET_CR_DATA<3>
52	CR_DATA4	ENET_CR_DATA<4>
53	CR_DATA5	ENET_CR_DATA<5>
54	CR_DATA6	ENET_CR_DATA<6>
55	CR_DATA7	ENET_CR_DATA<7>
59	CE*/MS_INS* (IPU-ENET)	NC_ENET_CE_L_MS_INS_L
60	CR_LED/ALE (IPU-ENET)	ENET_CR_PWREN
57	CR_WP*/XD_WP* (IPU-ENET)	
68	XD_DETECT (IPU-ENET)	ENET_SR_DISABLE

NOTE: "IPx" == Programmable pull-up/down

SD_DETECT can only be used active low due to errata.

Net	Resistor	Value
ENET_SD_DETECT_L	R3960	0
ENET_SD_CMD	R3961	33
ENET_SD_CLK	R3979	33
ENET_CR_DATA<0>	R3971	33
ENET_CR_DATA<1>	R3972	33
ENET_CR_DATA<2>	R3973	33
ENET_CR_DATA<3>	R3974	33
ENET_CR_DATA<4>	R3975	33
ENET_CR_DATA<5>	R3976	33
ENET_CR_DATA<6>	R3977	33
ENET_CR_DATA<7>	R3978	33

DEVELOPMENT, PLACEMENT_NOTE=PLACE NEAR U3900, 5% 1/16W MF-LF 402

SDCONN_DETECT_L, SDCONN_CMD, SDCONN_CLK, SDCONN_DATA<0>, SDCONN_DATA<1>, SDCONN_DATA<2>, SDCONN_DATA<3>, SDCONN_DATA<4>, SDCONN_DATA<5>, SDCONN_DATA<6>, SDCONN_DATA<7>

NC_ENET_CE_L_MS_INS_L NO_TEST=TRUE

No MS (Memory Stick) Insert feature needed. Control signal to light LED or control SD bus power.

SDCONN_WP

R3980 1K 5% 1/16W MF-LF 402 NOSTUFF — =PP3V3_S3_ENET_PHY_FET

R3981 1K 5% 1/16W MF-LF 402

ENET supports both active-levels for WP.

ENET 1.2V SR IS ENABLED IF FLOATING.

ENET_CR Signals

BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE

If ENET switching regulator is used, this pin can float (alias to TP_). If not used, must be pulled to 3.3V ENET via 1K resistor (not provided on this page).

R3965 1.24K 1% 1/16W MF-LF 402

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Avoids need for EFI to program at startup. (Required ROM size 1 Mbit)

=PP3V3_S3_ENET_PHY_FET

R3993 4.7K 5% 1/16W MF-LF 402

R3992 4.7K 5% 1/16W MF-LF 402

R3904 0 5% 402 1/16W MF-LF

U3990
AT45DB021D
SOIC-8S1
OMIT_TABLE

Pin	Signal	Net
8	VCC	
2	SCK	ENET_SCLK_R
4	CS*	ENET_CS_L
5	WP*	ENET_SWP_L
3	RESET*	ENET_SRESET_L
1	SI	ENET_MOSI
8	SO	ENET_MISO
	GND	

C3990 0.1UF 10% 16V X7R-CERM 402

NOSTUFF R3990 4.7K 5% 1/16W MF-LF 402

R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=K62 SYNC_DATE=01/06/2013

PAGE TITLE: ETHERNET PHY (CAESAR IV)

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

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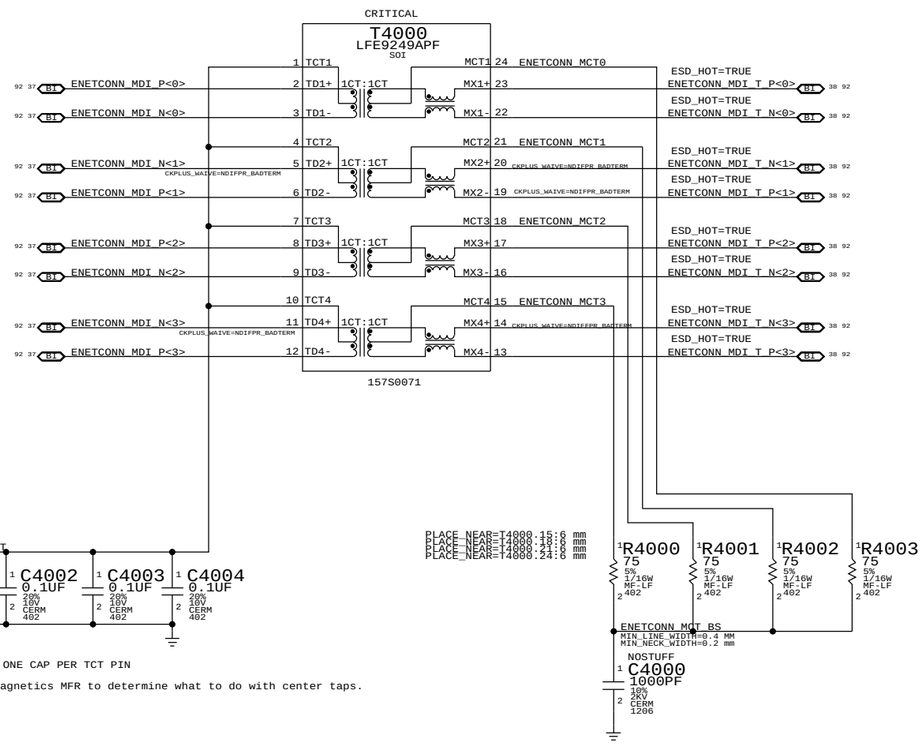
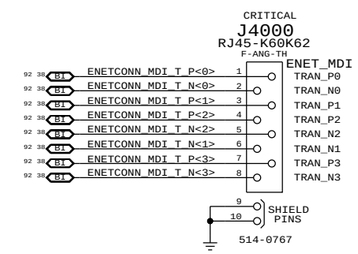
THIS PAGE DIFFERENT BETWEEN K60 and K62.



NOTE: Check with PHY and Magnetics MFR to determine what to do with center taps.

NOTE: BOB SMITH TERMINATION FOR EMC.

NO PAIR AND PIN POLARITY SWAPS



SYNC_MASTER=K60_MARK SYNC_DATE=01/06/2011

PAGE TITLE
Ethernet Connector

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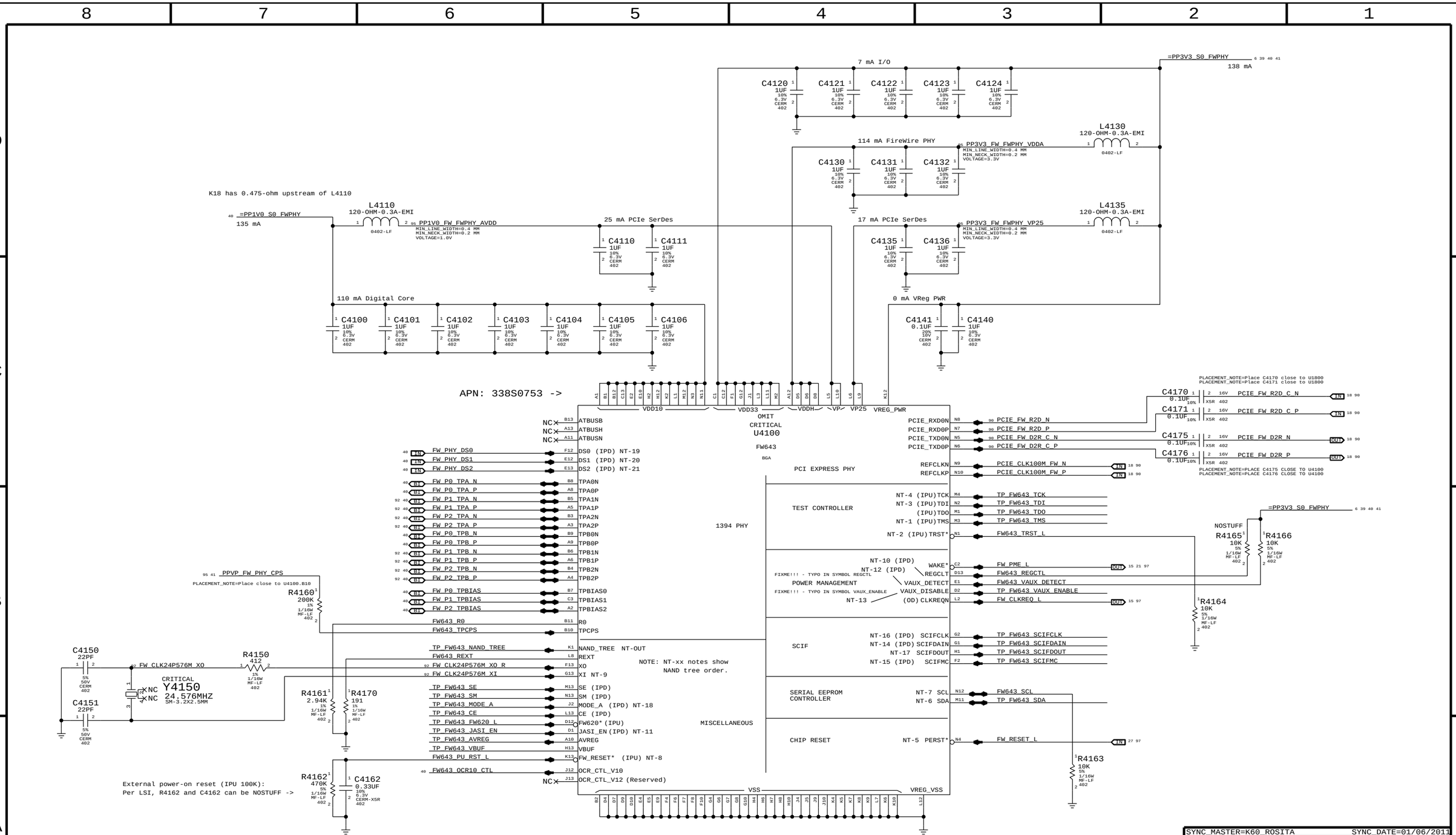

SYNC_MASTER=K60_ROSITA SYNC_DATE=01/06/2011

PAGE TITLE
FireWire LLC/PHY (FW643)

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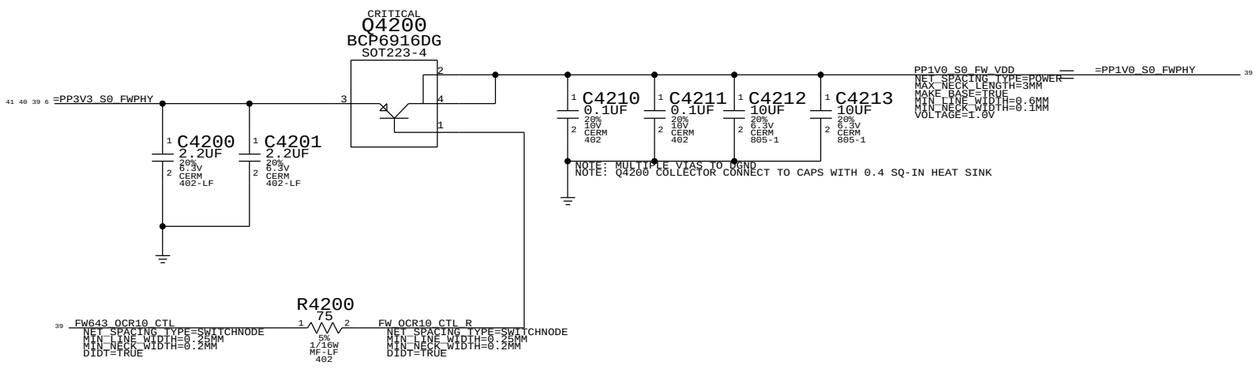
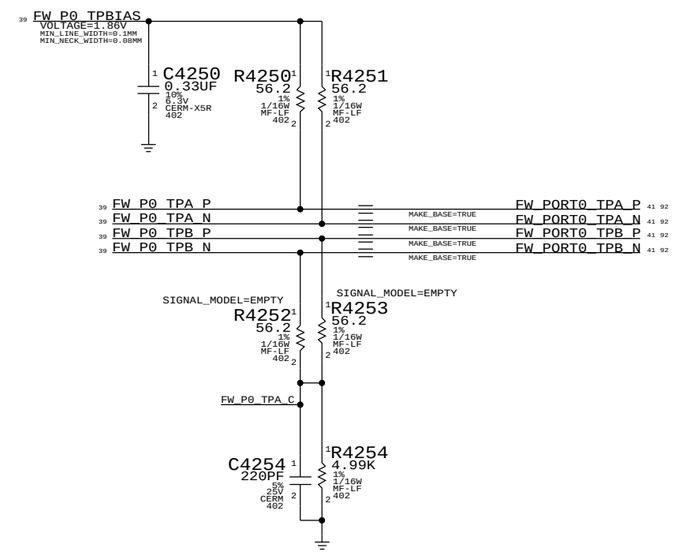
FW643 1.0V GENERATION

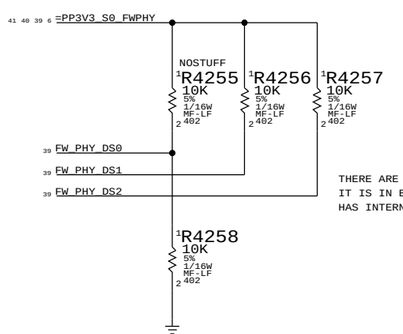


Termination

Place close to FireWire PHY



1394 PHY DATA/STROBE OPTIONS



THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE, FW643 HAS INTERNAL 100K PULL-DOWNS, ONLY PULL-UPS NECESSARY.

2ND & 3RD TPA/TPB PAIR UNUSED

39 FW_P1_TPBIAS		NC_FW_PORT1_TPBIAS
92 39 FW_P1_TPA_P		NC_FW_PORT1_TPA_P
92 39 FW_P1_TPA_N		NC_FW_PORT1_TPA_N
92 39 FW_P1_TPB_P		NC_FW_PORT1_TPB_P
92 39 FW_P1_TPB_N		NC_FW_PORT1_TPB_N
39 FW_P2_TPBIAS		NC_FW_PORT2_TPBIAS
92 39 FW_P2_TPA_P		NC_FW_PORT2_TPA_P
92 39 FW_P2_TPA_N		NC_FW_PORT2_TPA_N
92 39 FW_P2_TPB_P		NC_FW_PORT2_TPB_P
92 39 FW_P2_TPB_N		NC_FW_PORT2_TPB_N

MAKE_BASE=TRUE
NO_TEST=TRUE

NOTE: AGERE'S RECOMMENDATION FOR UNUSED PORTS

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
FireWire: 1394B MISC

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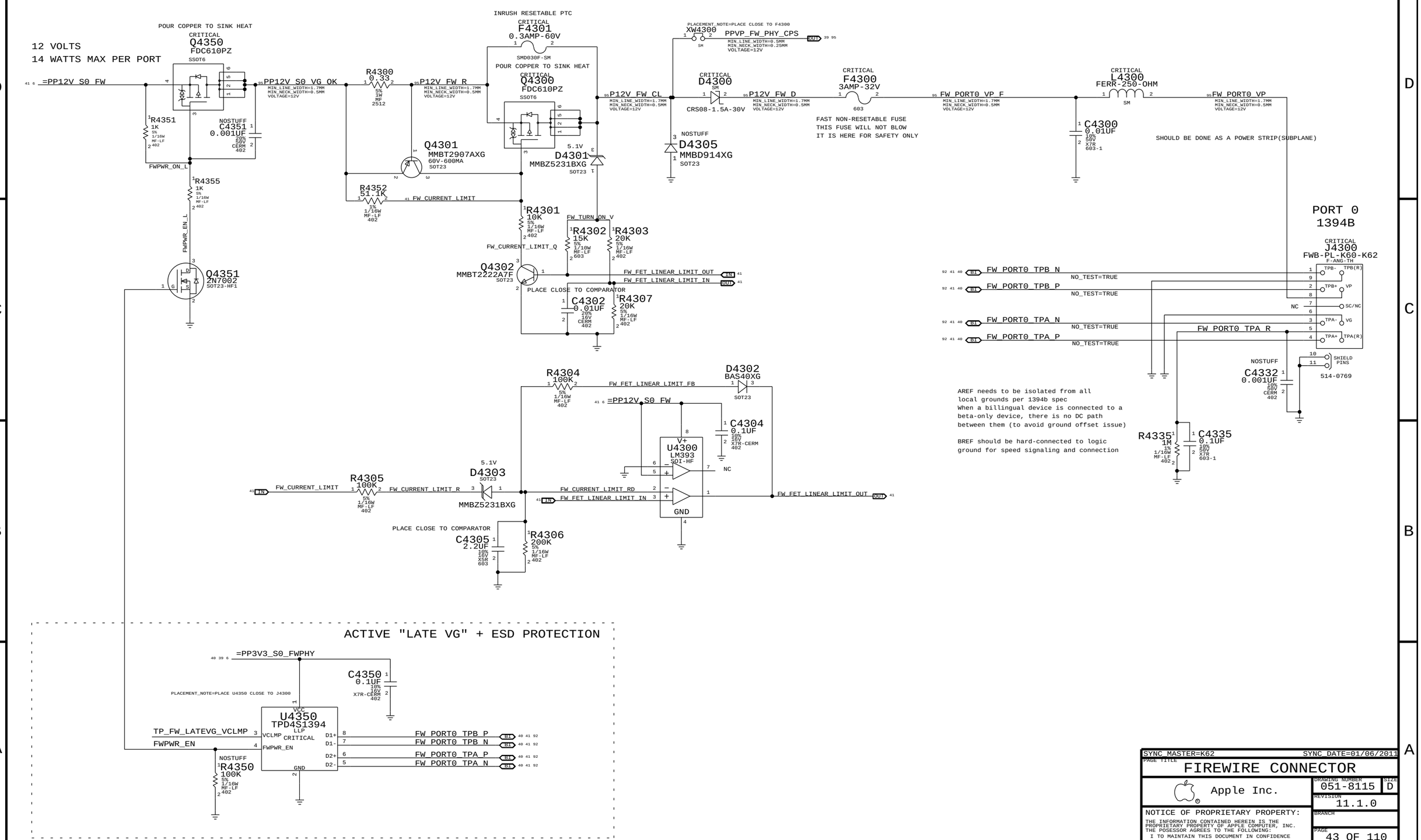

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
FIREWIRE CONNECTOR

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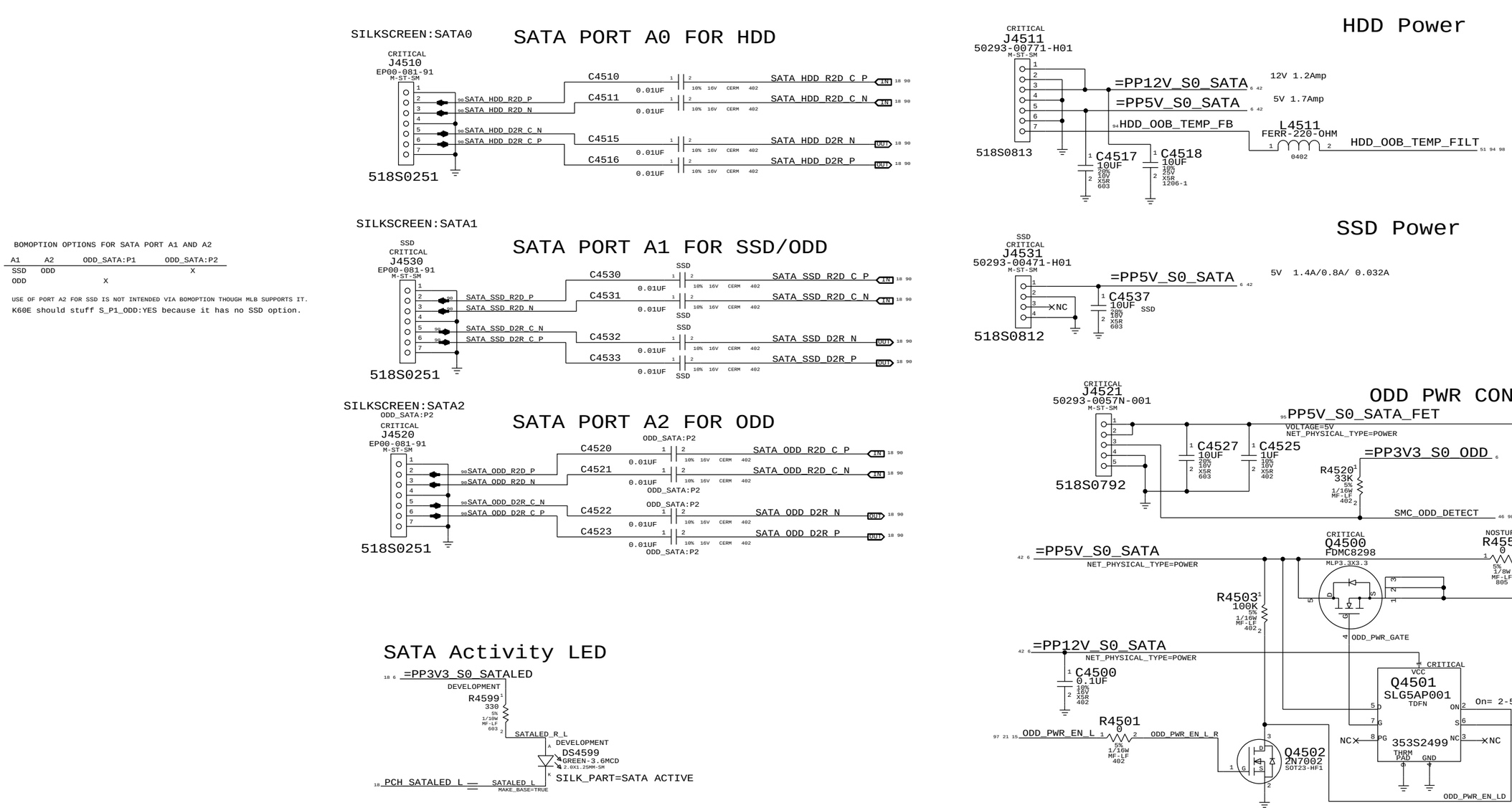

BOMOPTION OPTIONS FOR SATA PORT A1 AND A2

A1	A2	ODD_SATA:P1	ODD_SATA:P2
SSD	ODD		X
ODD		X	

USE OF PORT A2 FOR SSD IS NOT INTENDED VIA BOMOPTION THOUGH MLB SUPPORTS IT.
K60E should stuff S_P1_ODD:YES because it has no SSD option.

SYNC_MASTER=K60_JERRY SYNC_DATE=01/06/2011

PAGE TITLE: SATA Connectors

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DRAWING NUMBER: 051-8115 SIZE: D

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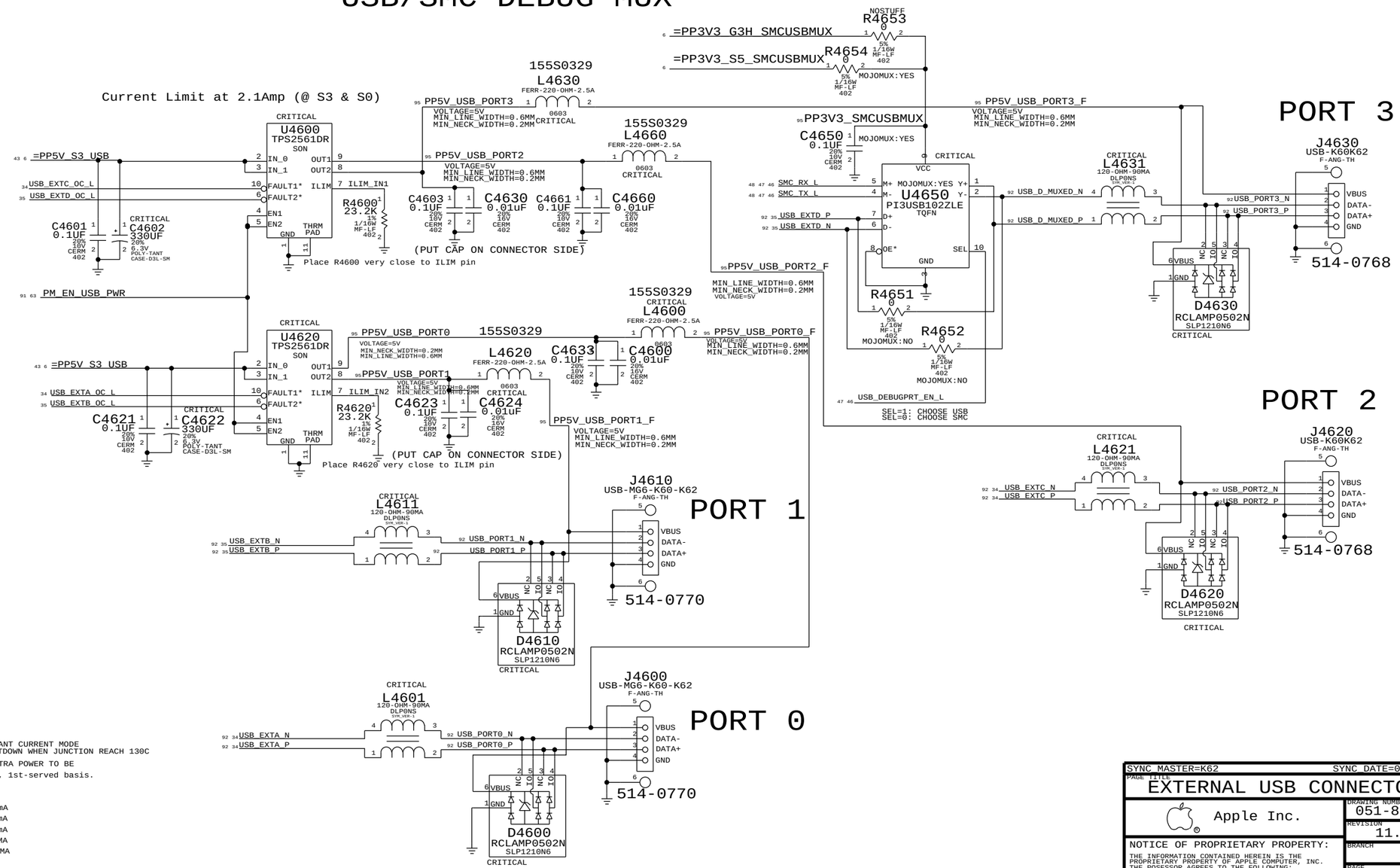
USB/SMC DEBUG MUX

ADDED AT EVT & SWITCH TO S5 RAIL



USB PORT POWER:

EACH PORT IS HARDWARE Capable of :

STATE	MAX	MIN (WITHIN THE TOLERANCE)
S0, S3	2.7A	2.1A -- PER PORT

WHEN CURRENT HITS LIMIT, TPS2561 BECOME CONSTANT CURRENT MODE AND STAY AT THE LIMIT LEVEL UNTIL THERMAL SHUTDOWN WHEN JUNCTION REACH 130C

SOFTWARE WILL ALOW 500MA/PORT, PLUS 2700MA EXTRA POWER TO BE distributed to approved devices on a 1st-come, 1st-served basis.

EXAMPLE: Port 1 - iPad fast charging = 2100mA
Port 2 - Wired Keyboard = 1100mA
Port 3 - iPhone fast charging = 1000mA
PORT 4 - USB 2.0 500MA = 500MA
TOTAL: 4700MA

SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE
EXTERNAL USB CONNECTORS

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
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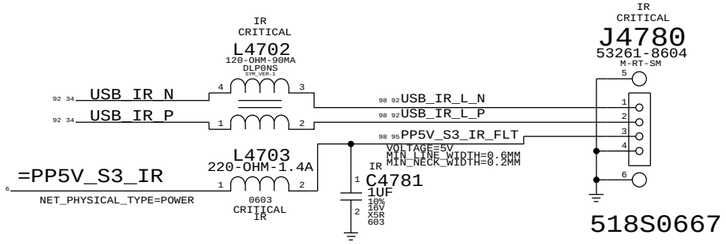
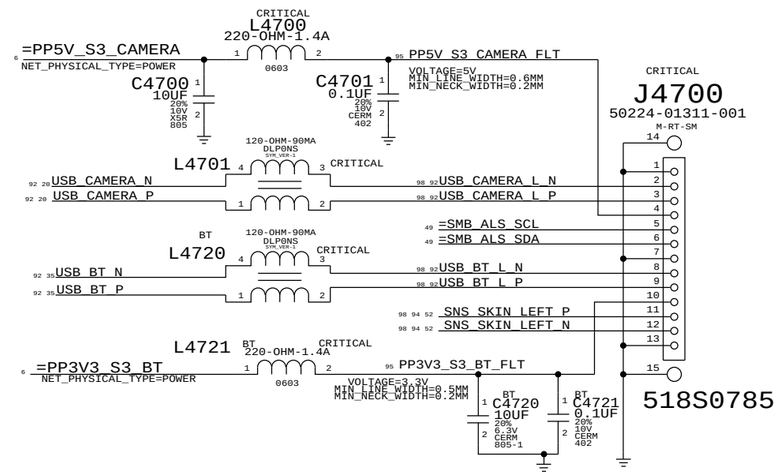
IR RECEIVER CONNECTOR

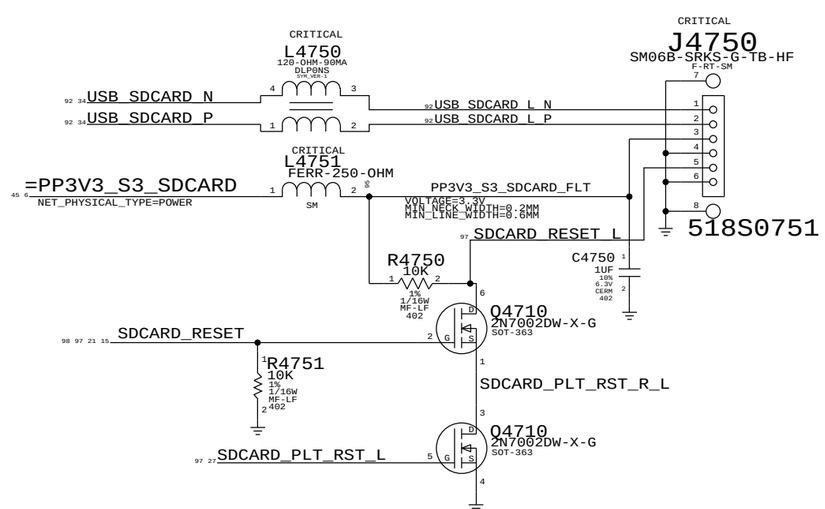


CAMERA/ALS & BLUETOOTH (K37A) CONNECTOR



Skin Temp sense at upper Left Screen corner

SD Card Reader Board (Lazarus)



SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
Internal USB Connections

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

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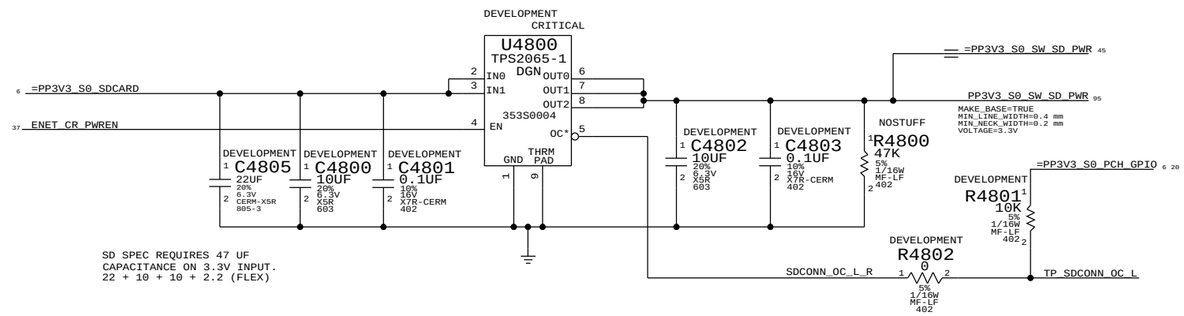
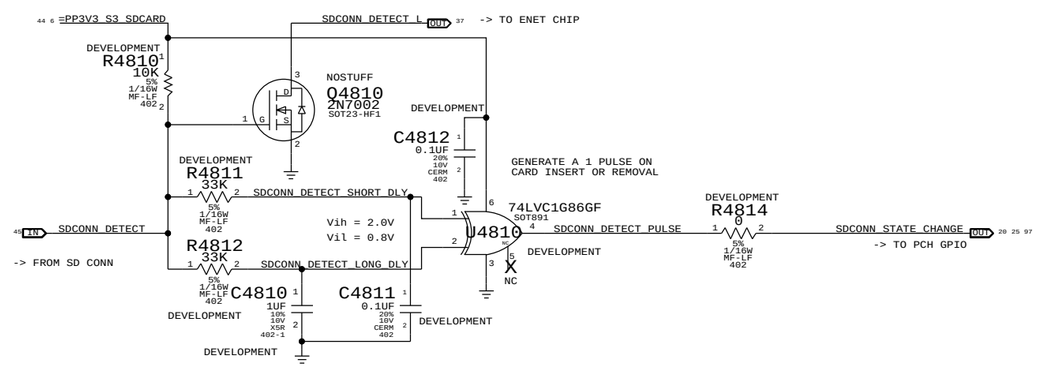
SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

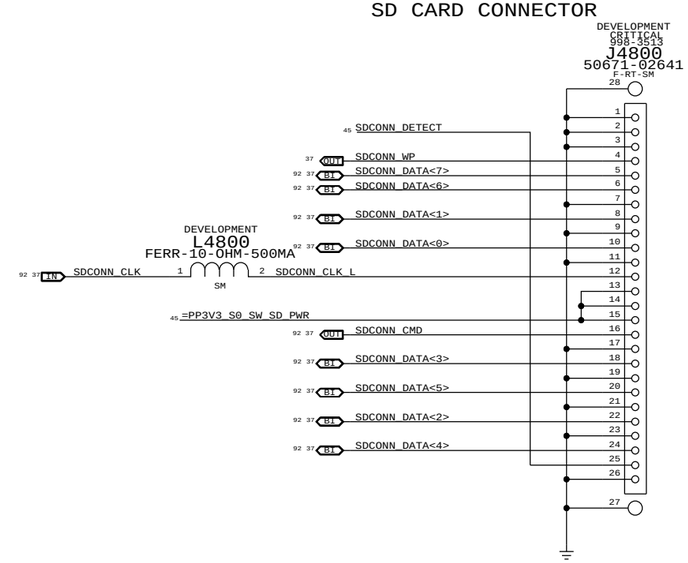
TPS2065-1 (1.0A LIMIT) HAS ACTIVE LOAD DISCHARGE SO R4800 IS NOSTUFF.



SDCONN DETECT DEBOUNCE, INVERSION, AND DETECT-CHANGED PCH GPIO CIRCUIT



SD CARD CONNECTOR



(CARD INSERTED = OPEN)
CAESAR-IV CARD DETECT IS PROGRAMMABLE, BUT A SILICON BUG
MAKES THE ACTIVE-HIGH CASE UNUSABLE.

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
SD READER CONNECTOR

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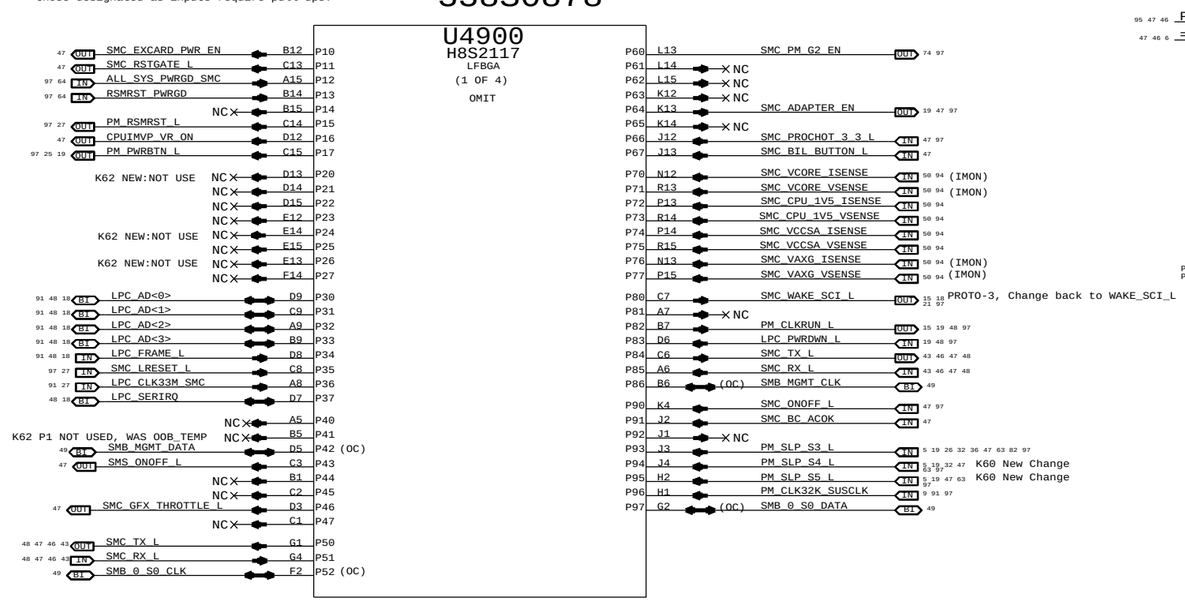
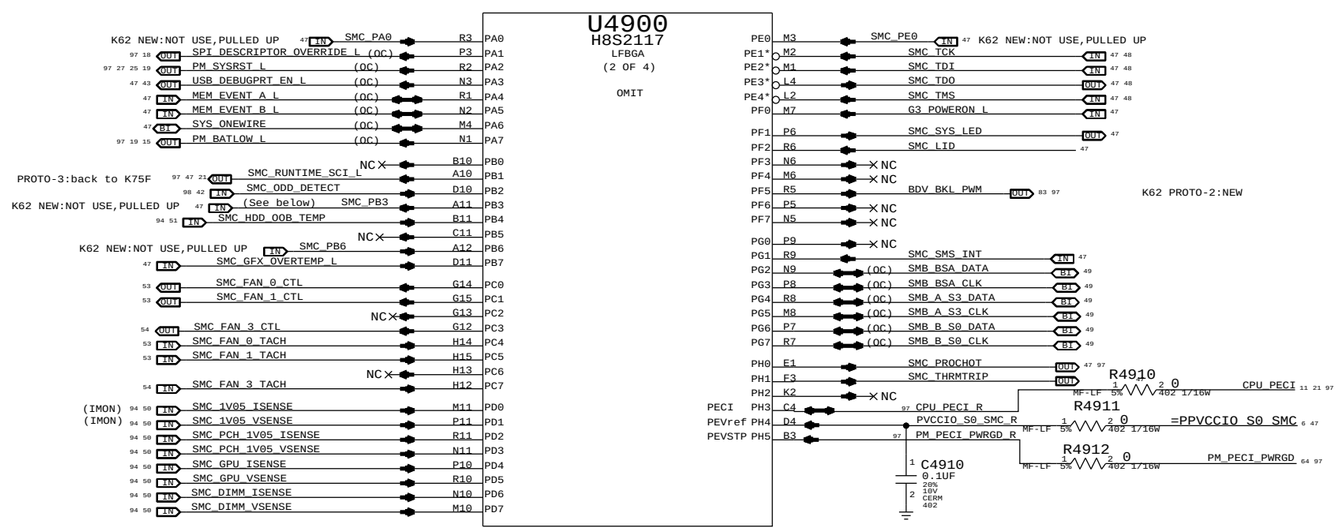
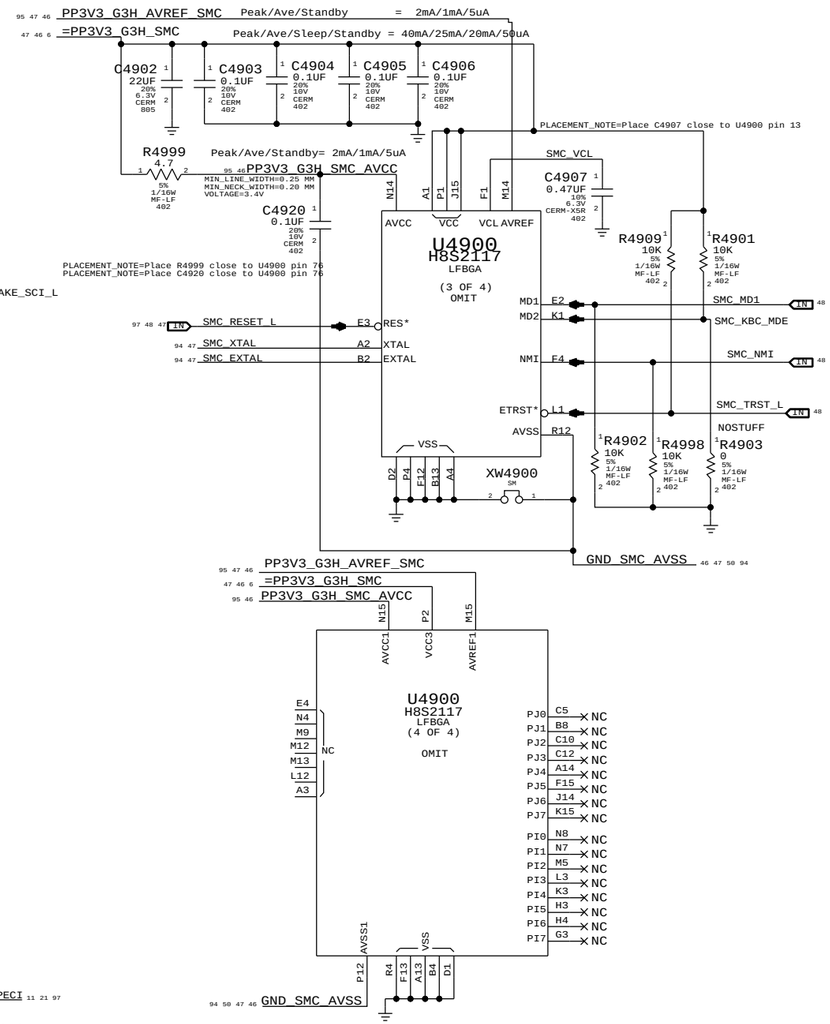
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designed as inputs require pull-ups.

338S0878







SMC PB3: SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

SMC PG1: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC MASTER=K62	SYNC DATE=01/06/2011
PAGE TITLE: SMC	
Apple Inc.	DRAWING NUMBER: 051-8115 — SIZE: D
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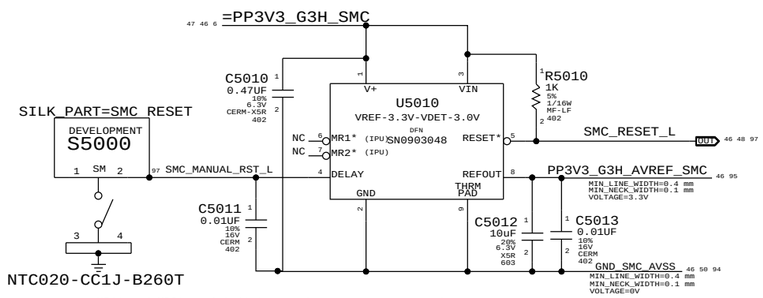
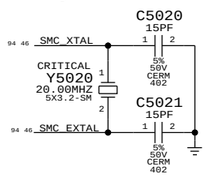
SMC Reset "Button", Supervisor & AVREF Supply



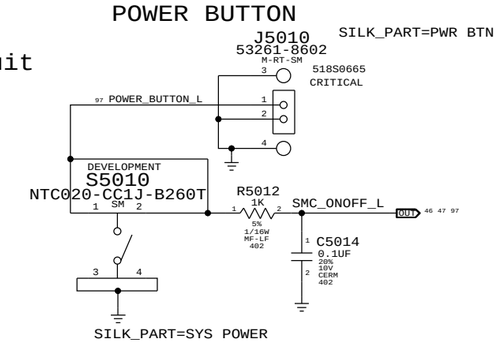
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

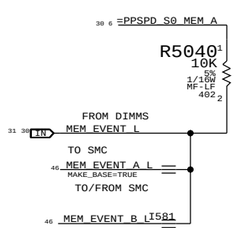
SMC Crystal Circuit



POWER BUTTON



MEM_EVENT



MISC. SIGNAL ALIASES

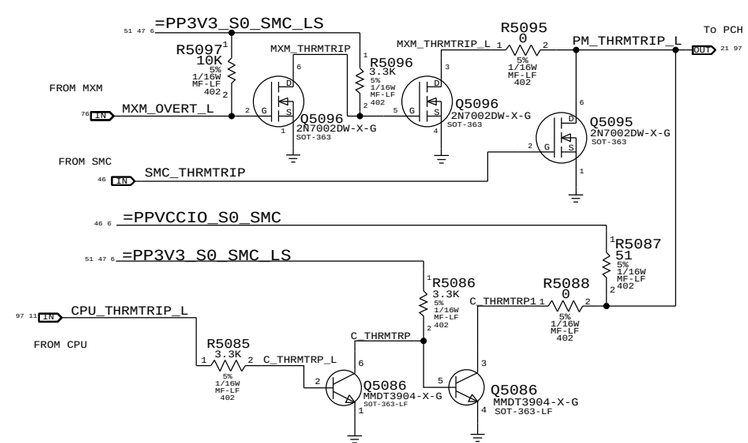
SMC_GFX_OVERTEMP_L	MXM_ALERT_L	MAKE_BASE=TRUE
SMC_GFX_THROTTLE_L	MXM_PWR_LEVEL	MAKE_BASE=TRUE
CPUIMVP_VR_ON	SMC_DELAYED_PWRGD	MAKE_BASE=TRUE

UNUSED PORT 7 ANALOG SENSORS

UNUSED TP/NC ALIASES

SMC_EXCARD_PWR_EN	TP_SMC_EXCARD_PWR_EN	MAKE_BASE=TRUE
SMS_ONOFF_L	TP_SMS_ONOFF_L	MAKE_BASE=TRUE
SMC_RSTGATE_L	TP_SMC_RSTGATE_L	MAKE_BASE=TRUE
SMC_SYS_LED	TP_SMC_SYS_LED	MAKE_BASE=TRUE
SMC_PB3	TP_SMC_PB3	MAKE_BASE=TRUE

SMC & MXM THERMTRIP LEVEL SHIFTING



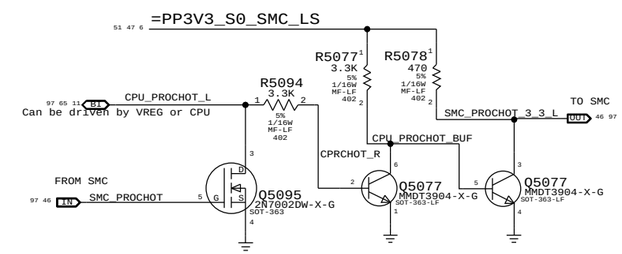
=PP3V3_G3H_SMC

SMC_ONOFF_L	R5020	10K	5%	1/16W MF-LF 402
SMC_TX_L	R5021	10K	5%	1/16W MF-LF 402
SMC_RX_L	R5022	100K	5%	1/16W MF-LF 402
SYS_ONEWIRE	R5023	2.0K	5%	1/16W MF-LF 402
SMC_TMS	R5024	10K	5%	1/16W MF-LF 402
SMC_TDO	R5025	10K	5%	1/16W MF-LF 402
SMC_TDI	R5026	10K	5%	1/16W MF-LF 402
SMC_TCK	R5027	10K	5%	1/16W MF-LF 402
SMC_BIL_BUTTON_L	R5028	10K	5%	1/16W MF-LF 402
SMC_BC_ACOK	R5029	10K	5%	1/16W MF-LF 402
SMC_ADAPTER_EN	R5030	10K	5%	1/16W MF-LF 402
USB_DEBUGPRT_EN_L	R5031	10K	5%	1/16W MF-LF 402
G3_POWERON_L	R5034	10K	5%	1/16W MF-LF 402
SMC_SMS_INT	R5032	10K	5%	1/16W MF-LF 402
SMC_LID	R5033	10K	5%	1/16W MF-LF 402
SMC_PA0	R5037	100K	5%	1/16W MF-LF 402
SMC_PB6	R5038	100K	5%	1/16W MF-LF 402
SMC_PE0	R5036	100K	5%	1/16W MF-LF 402

=PP3V3_S0_SMC_LS

SMC_GFX_OVERTEMP_L	R5035	10K	5%	1/16W MF-LF 402
SMC_RUNTIME_SCI_L	R5044	10K	5%	1/16W MF-LF 402
PM_SLP_S3_L	R5041	100K	5%	1/16W MF-LF 402
PM_SLP_S5_L	R5042	100K	5%	1/16W MF-LF 402
PM_SLP_S4_L	R5043	100K	5%	1/16W MF-LF 402

SMC PROCHOT 3.3V LEVEL SHIFTING



SYNC_MASTER=K62	SYNC_DATE=01/06/2011
PAGE TITLE	SMC Support
Apple Inc.	DRAWING NUMBER 051-8115 SIZE D
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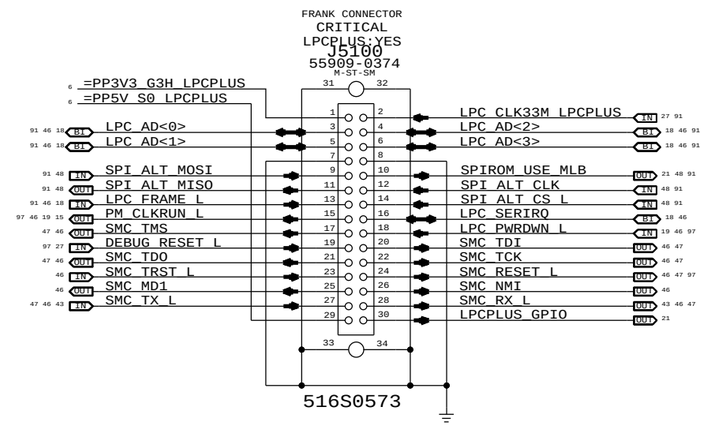
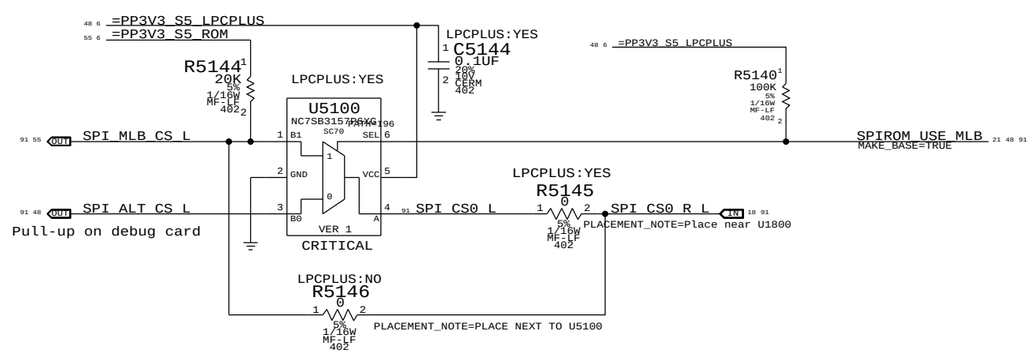
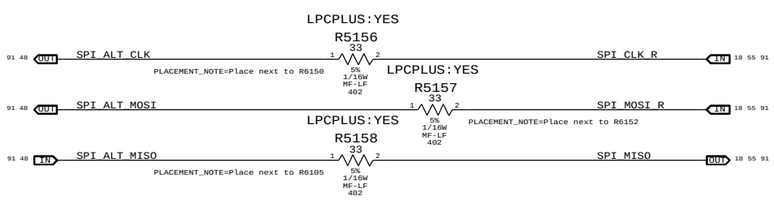
LPC+SPI Connector



Alternate SPI ROM Support



SPI Bus Series Resistance Option



SYNC_MASTER=K62_AARON SYNC_DATE=11/30/2009

PAGE TITLE
LPC+SPI Debug Connector

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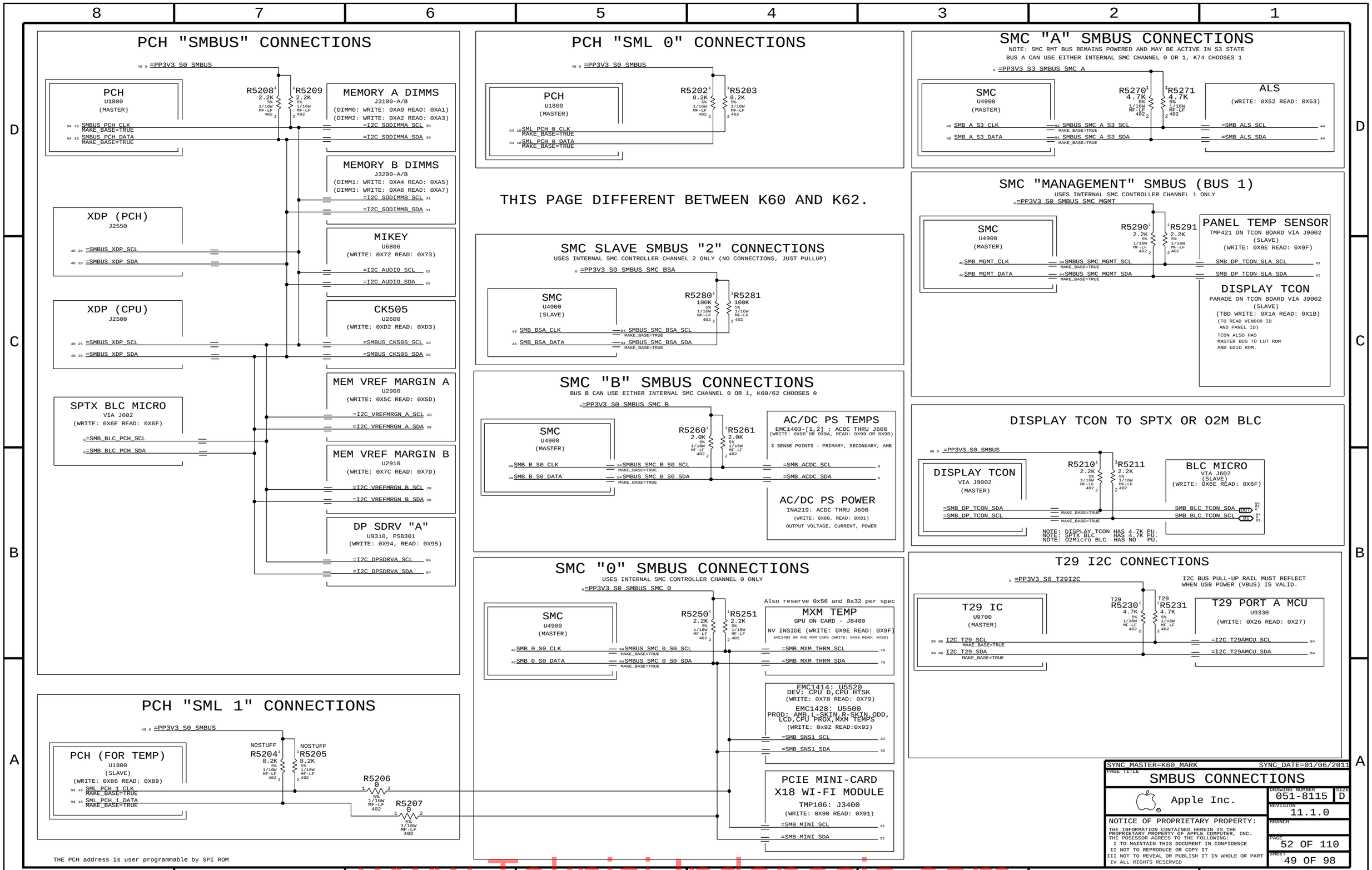

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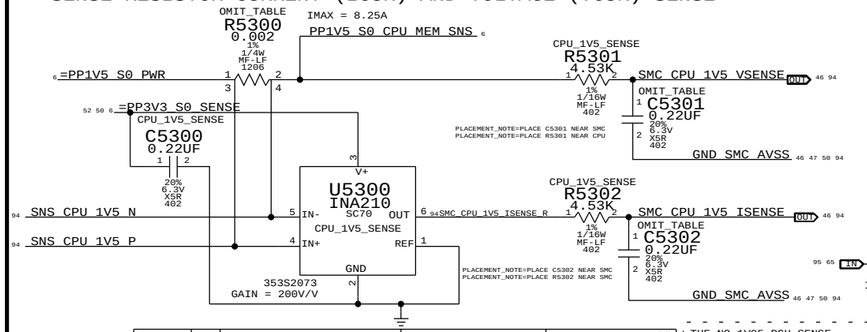
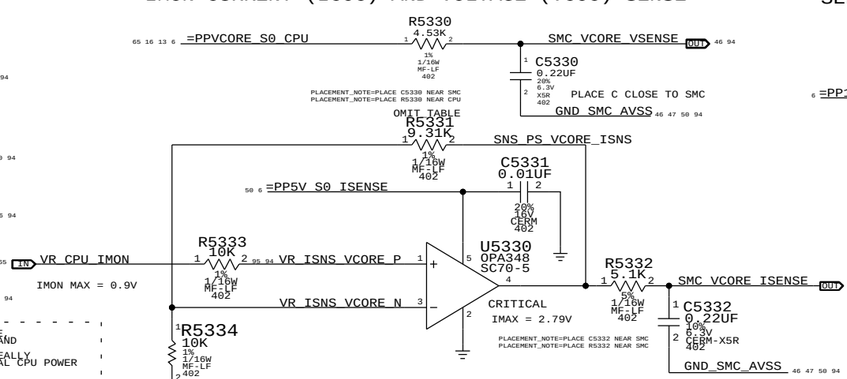
CPU VDD 1.5V
SENSE RESISTOR CURRENT (IC5R) AND VOLTAGE (VC5R) SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5300	CPU_1V5_SENSE
101S0414	1	RES,0 OHM,1206,20 MILLIOHM MAX	R5300	NO_CPU_1V5_SENSE
132S0080	2	CAP,0.22UF,402	C5301,C5302	CPU_1V5_SENSE
116S0004	2	RES,0 OHM,402	C5301,C5302	NO_CPU_1V5_SENSE

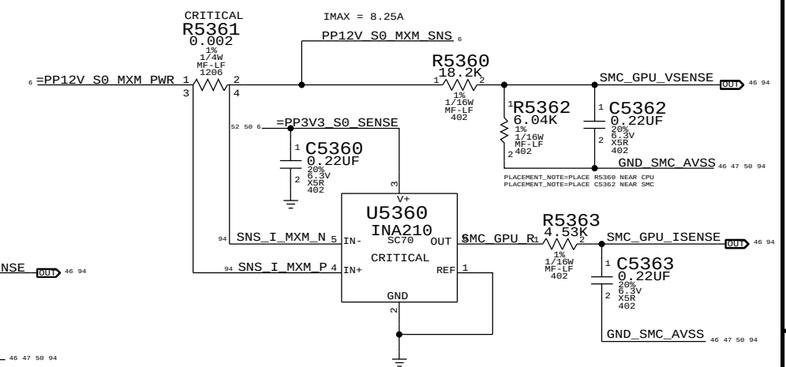
THE NO_1V05_PCH_SENSE, NO_CPU_VCCSA_SENSE, AND NO_CPU_1V5_SENSE BOMOPTIONS SHOULD IDEALLY NEVER BE USED AS TOTAL CPU POWER SENSING REQUIRES ALL 3 SENSORS.

CPU VCC (VCORE)
IMON CURRENT (IC0C) AND VOLTAGE (VC0C) SENSE

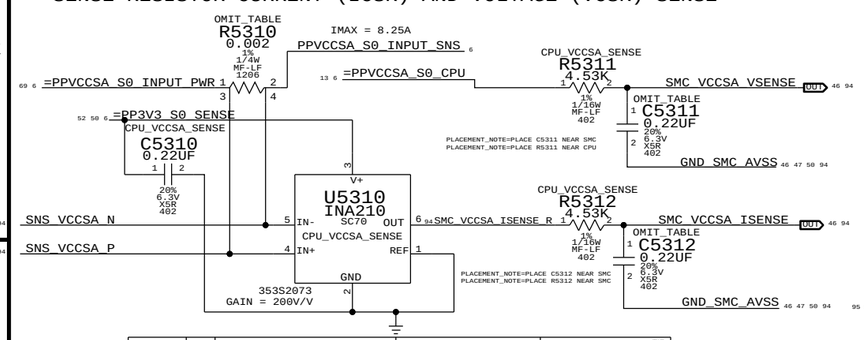


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0312	1	RES,MTL FILM,1/16W,9.31K,0402	R5331	CPUVCORE-3PH
114S0345	1	RES,MTL FILM,1/16W,21K,0402	R5331	CPUVCORE-4PH

GPU MXM
SENSE RESISTOR CURRENT (IG0R) AND VOLTAGE (VG0R) SENSE

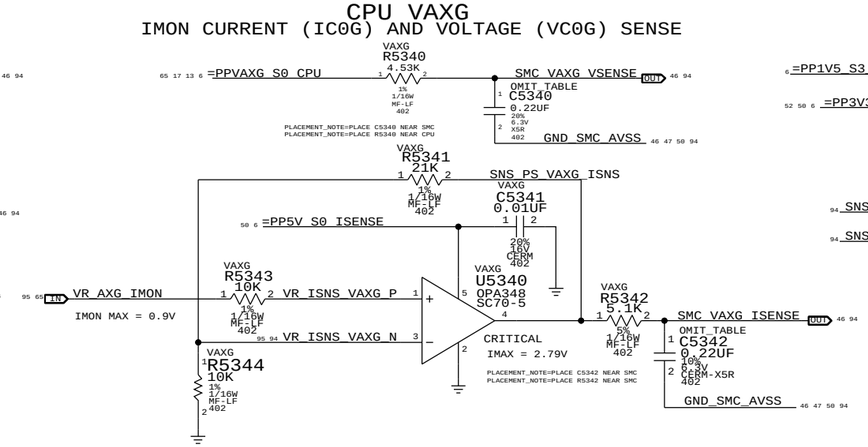


CPU VCCSA
SENSE RESISTOR CURRENT (ICSR) AND VOLTAGE (VCSR) SENSE



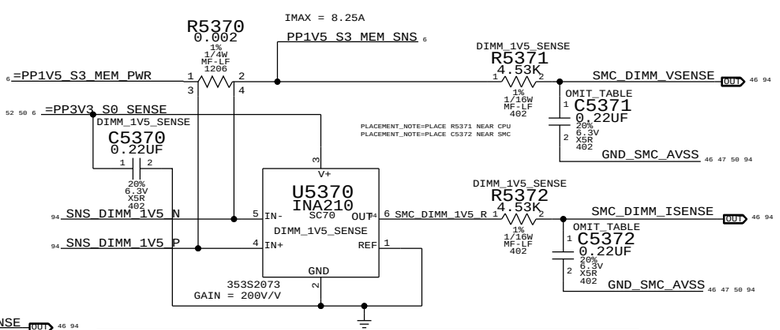
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5310	CPU_VCCSA_SENSE
101S0414	1	RES,0 OHM,1206,20 MILLIOHM MAX	R5310	NO_CPU_VCCSA_SENSE
132S0080	2	CAP,0.22UF,402	C5311,C5312	CPU_VCCSA_SENSE
116S0004	2	RES,0 OHM,402	C5311,C5312	NO_CPU_VCCSA_SENSE

CPU VAXG
IMON CURRENT (IC0G) AND VOLTAGE (VC0G) SENSE



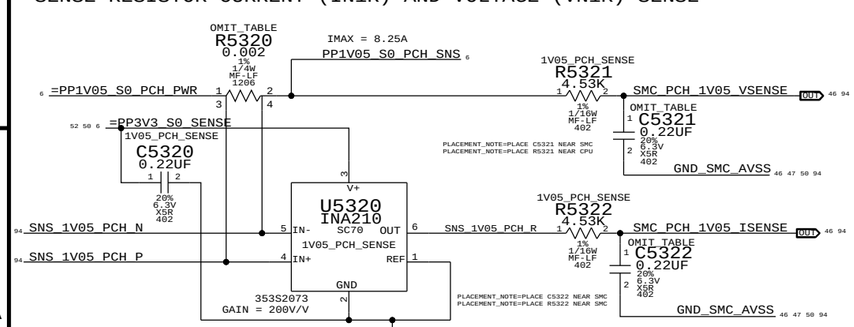
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	2	CAP,0.22UF,402	C5340,C5342	VAXG
116S0004	2	RES,0 OHM,402	C5340,C5342	NO_VAXG

DIMM VDD 1.5V (LIKELY DEVELOPMENT ONLY)
SENSE RESISTOR CURRENT (IM0R) AND VOLTAGE (VM0R) SENSE



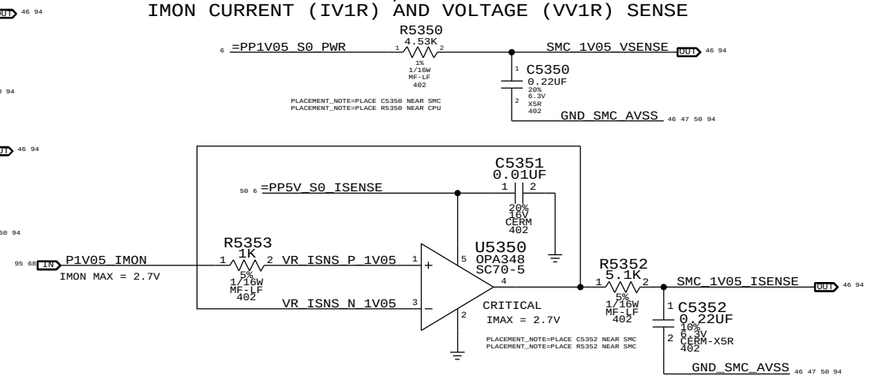
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	2	CAP,0.22UF,402	C5371,C5372	DIMM_1V5_SENSE
116S0004	2	RES,0 OHM,402	C5371,C5372	PRODUCTION

PCH 1.05V
SENSE RESISTOR CURRENT (IN1R) AND VOLTAGE (VN1R) SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5320	1V05_PCH_SENSE
101S0414	1	RES,0 OHM,1206,20 MILLIOHM MAX	R5320	NO_1V05_PCH_SENSE
132S0080	2	CAP,0.22UF,402	C5321,C5322	1V05_PCH_SENSE
116S0004	2	RES,0 OHM,402	C5321,C5322	NO_1V05_PCH_SENSE

1.05V FOR CPU VCCIO, CPU VCCSA & PCH 1.05V
IMON CURRENT (IV1R) AND VOLTAGE (VV1R) SENSE



NOTE: TOTAL CPU POWER = VC0C*ICOC + VC5R*IC5R + VC5R*ICSR + VC0G*IC0G + VV1R*ICIR
where ICIR = IV1R - IN1R - ICSR

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
CPU/PCH/GPU POWER SENSE

Apple Inc.

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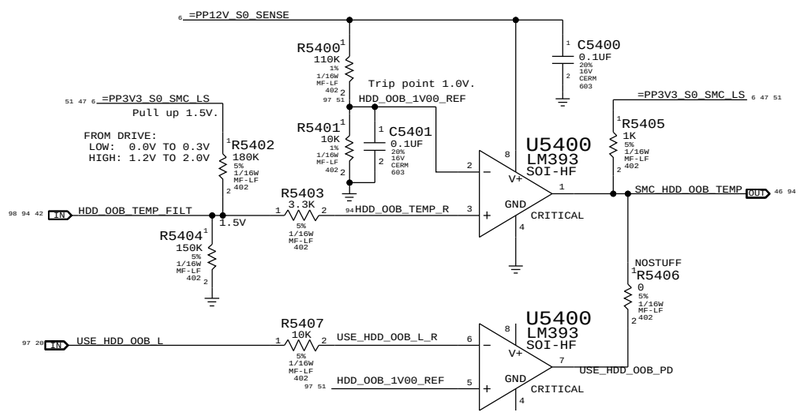
HDD OOB TEMPERATURE SENSING



DRIVE ACTIVE = VALID SIGNAL PROTOCOL BETWEEN 0-2.0V.
DRIVE ASLEEP = HDD DRIVES HDD_OOB_TEMP LOW
DRIVE ABSENT = OOB IS PULLED HIGH UNLESS PCH DETERMINES SSD PRESENT AND DRIVES USE_HDD_OOB_L LOW WHICH THEN PULLS HDD_OOB_TEMP LOW.

NOTE: WILL BE CONNECTED TO SATA PWR CONNECTOR PIN 11
THIS PIN IS ORIGINALLY INTENDED FOR HDD LED OUTPUT,
AND ALSO FOR HDD STAGGERED PIN UP (FLOATING) OR IMMEDIATE SPIN-UP (GROUND).
BOTH FUNCTIONS NOT USED.

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
HDD OOB SENSE

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DRAWING NUMBER 051-8115 SIZE D
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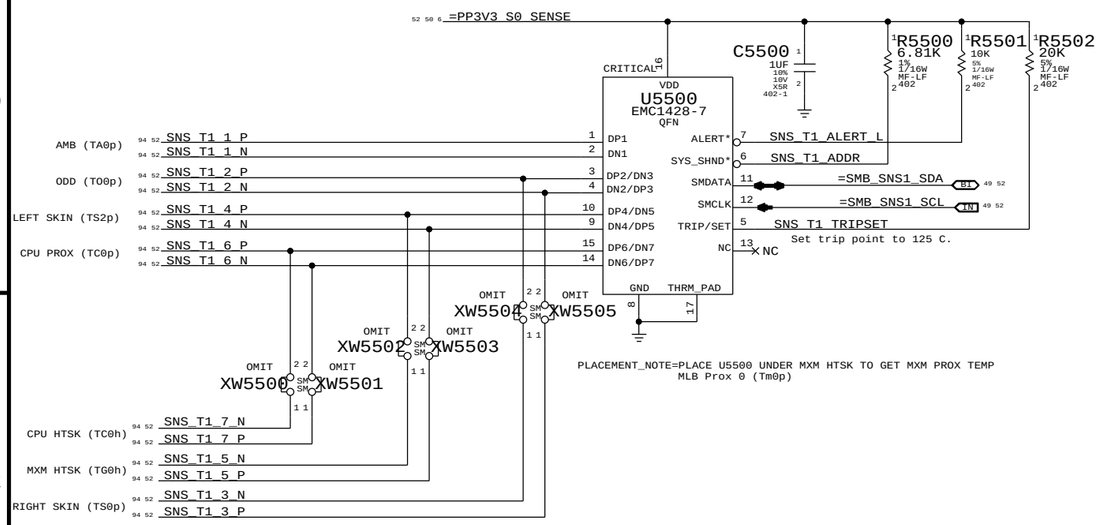
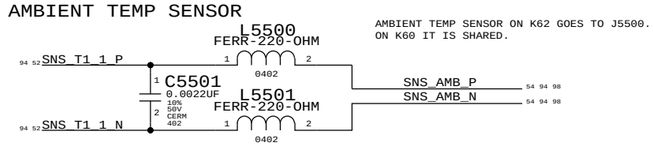
SNS T1: PRODUCTION TEMP SENSOR IC



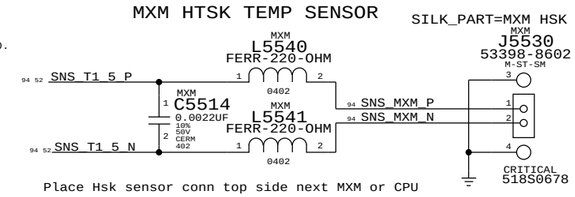
EMC1428-7: 6.8K PULL UP: I2C ADDRESS: WRITE: 0x92, READ: 0x93

AMBIENT TEMP SENSOR



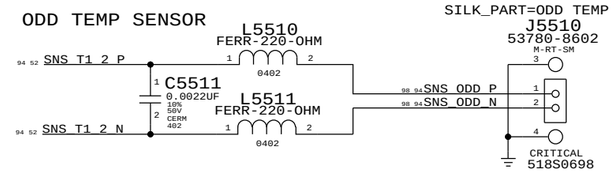
AMBIENT TEMP SENSOR ON K62 GOES TO J5500.
ON K60 IT IS SHARED.

MXM HTSK TEMP SENSOR

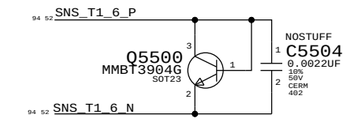


Place Hsk sensor conn top side next MXM or CPU

ODD TEMP SENSOR

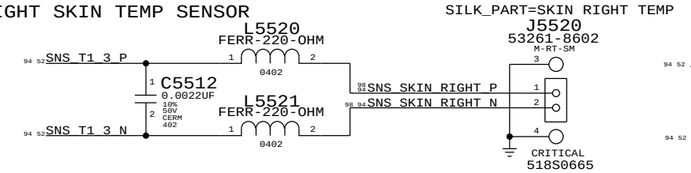


CPU PROXIMITY TEMP SENSOR

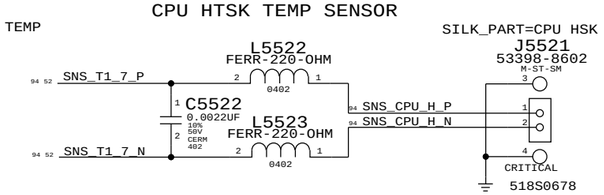


Place Q5500 (CPU Proximity Sensor) at the solder side
at edge near backer plate of CPU to replace HeatSink Temp Sensor

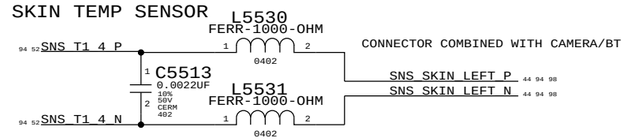
RIGHT SKIN TEMP SENSOR



CPU HTSK TEMP SENSOR

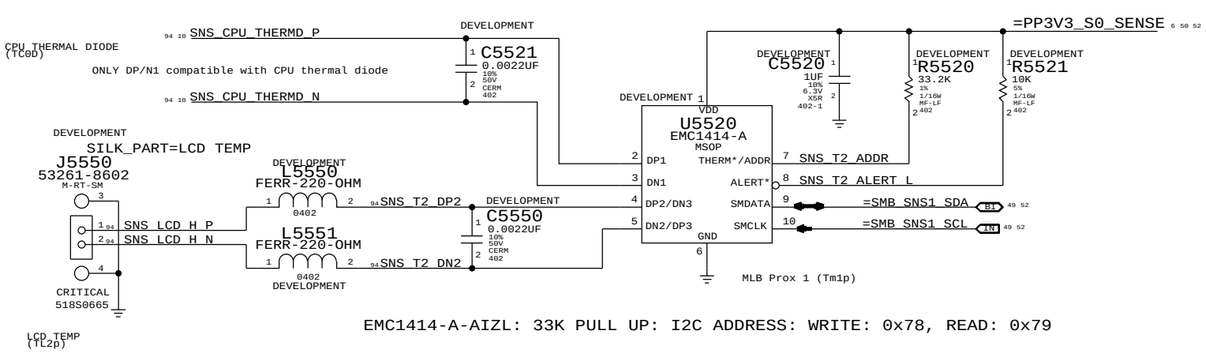


LEFT SKIN TEMP SENSOR



THIS PAGE DIFFERENT BETWEEN K60 AND K62.

SNS T2: DEVELOPMENT TEMP SENSOR IC



EMC1414-A-AIZL: 33K PULL UP: I2C ADDRESS: WRITE: 0x78, READ: 0x79

SYNC MASTER=K60_MARK	SYNC DATE=01/06/2011
PAGE TITLE: TEMP SENSORS	
Apple Inc.	DRAWING NUMBER 051-8115 SIZE D
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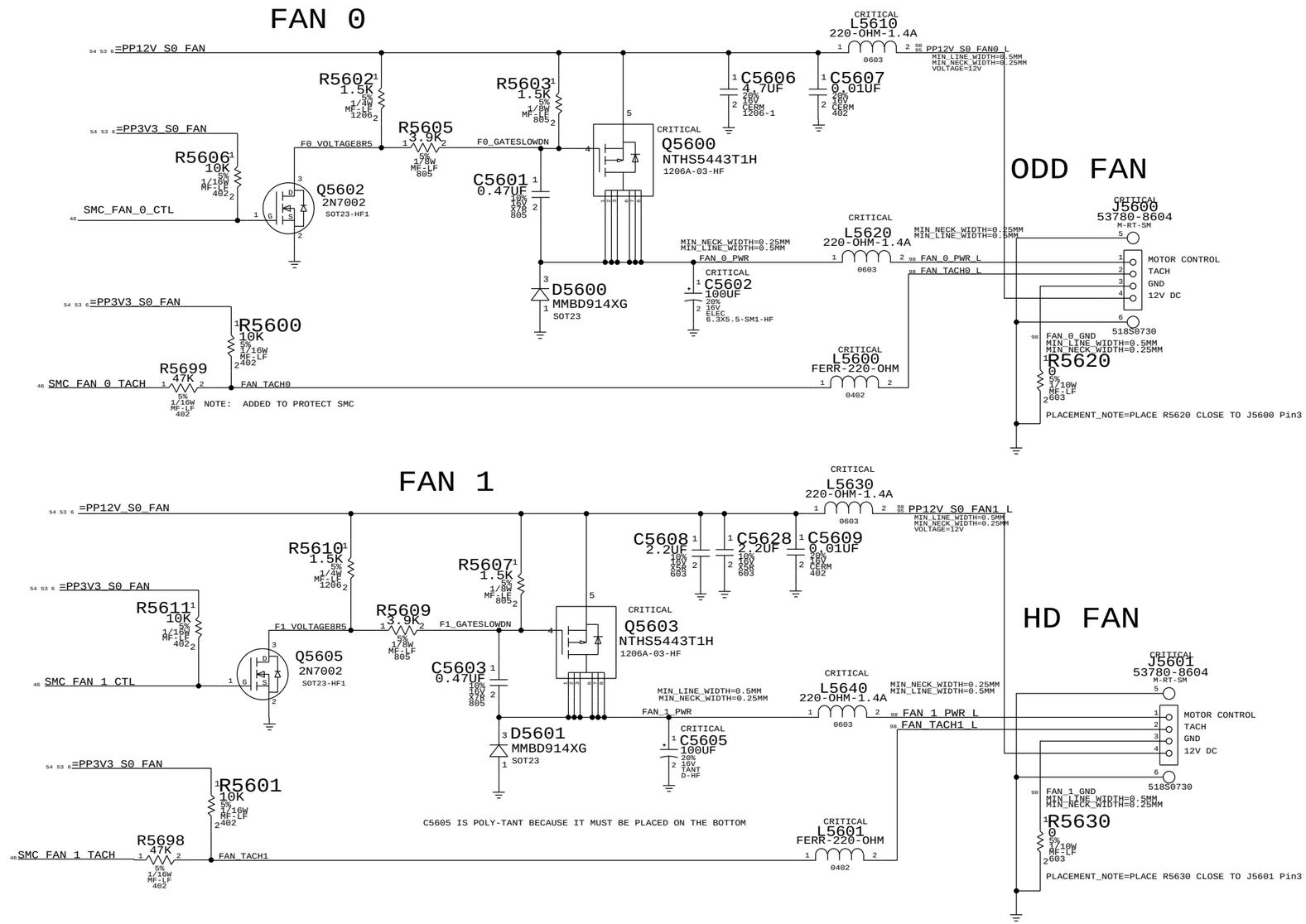

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: HD AND OD FAN

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DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

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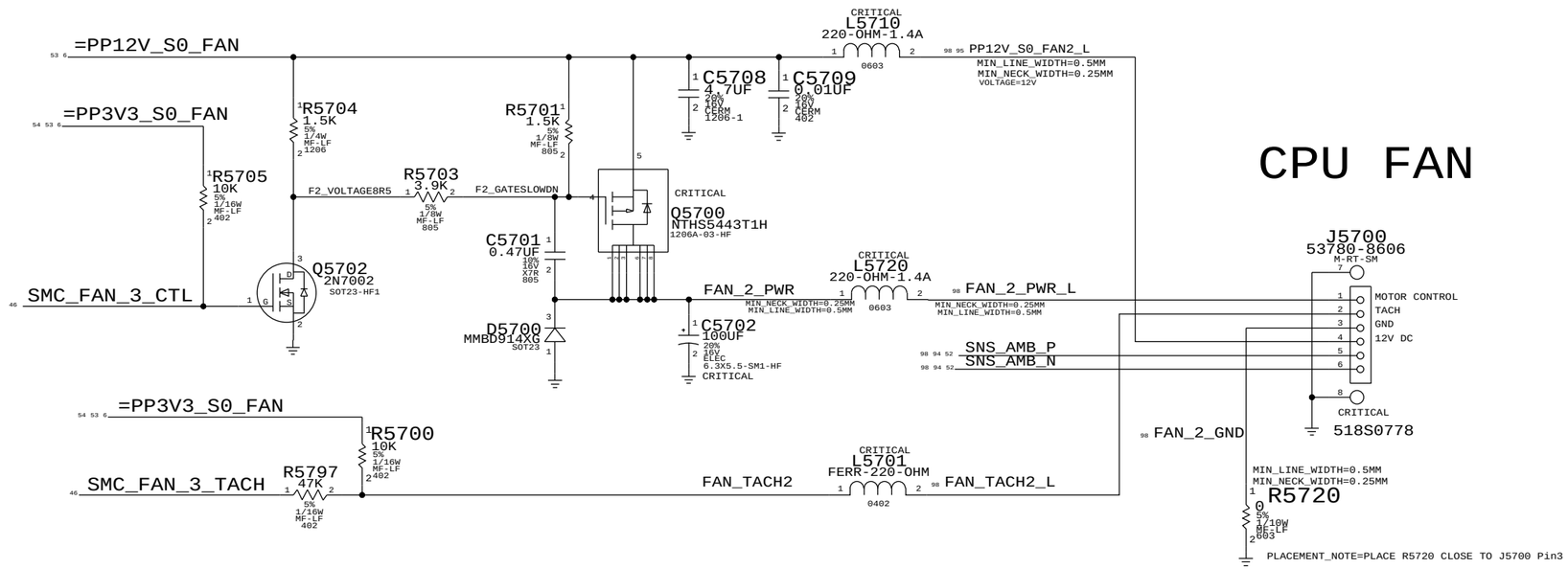
SMC'S FAN3 OUTPUT CONTROL FAN 2



CPU FAN

FAN 3 SMC CONTROL (UNUSED)

SYNC_MASTER=K60_JERRY	SYNC_DATE=01/06/2011
PAGE TITLE: CPU FAN	
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	REVISION: 11.1.0
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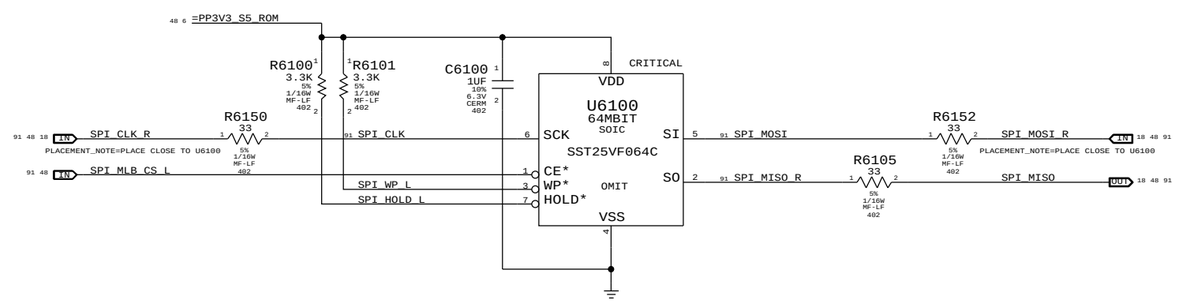

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PAGE TITLE

SPI ROM

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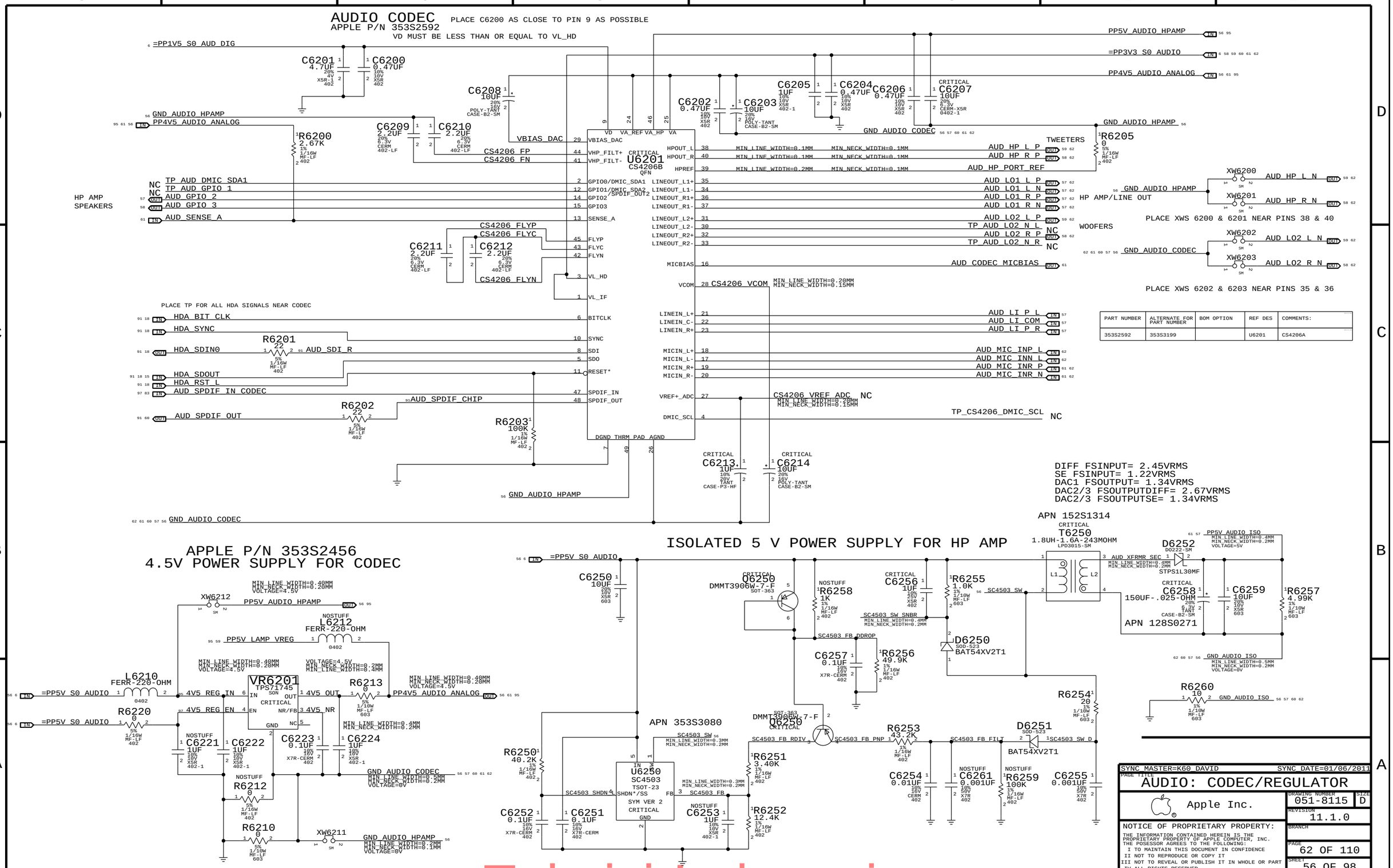

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S2592	353S3199		U6201	CS4206A

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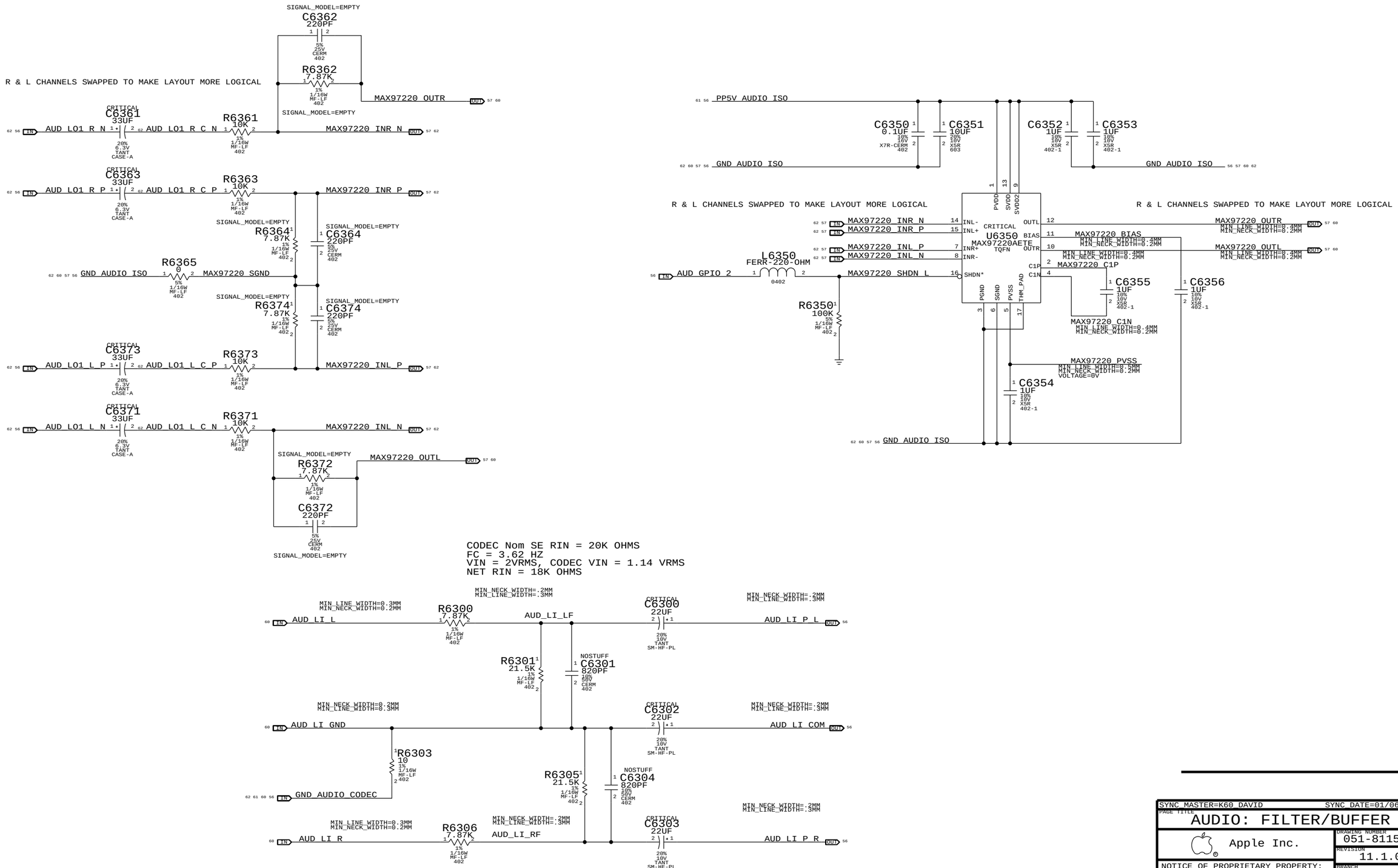

SYNC_MASTER=K60_DAVID SYNC_DATE=01/06/2011

PAGE TITLE
AUDIO: FILTER/BUFFER

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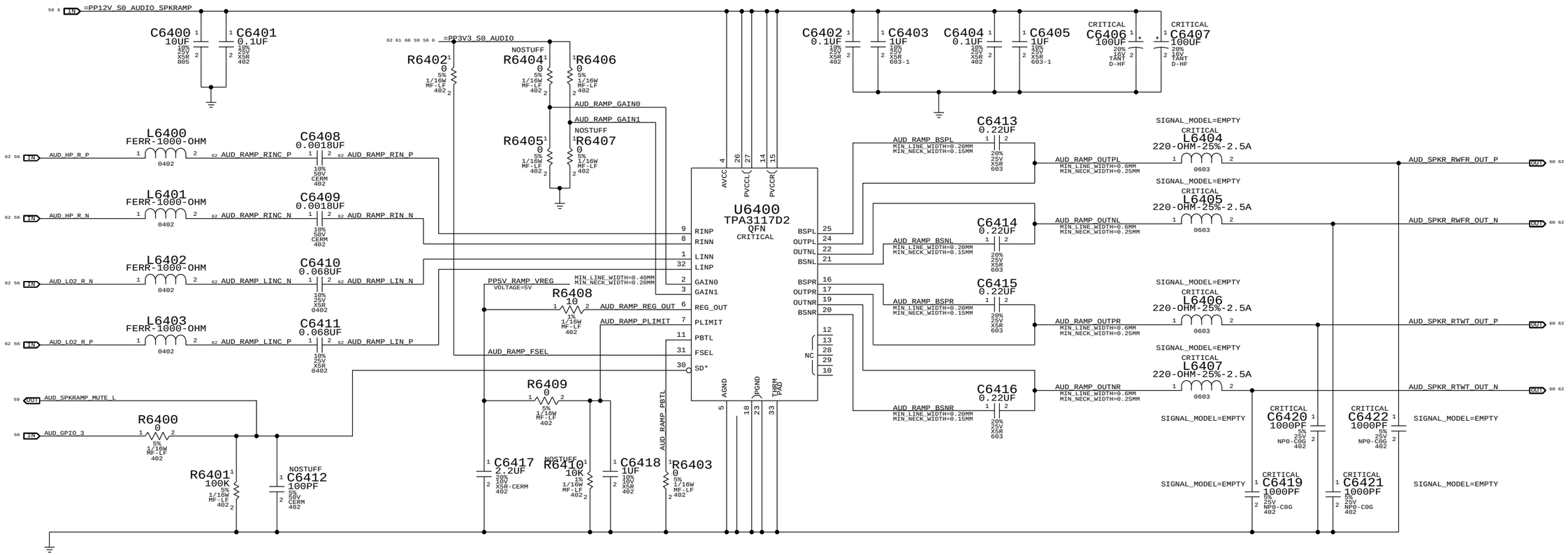
RIGHT CH SPEAKER AMP

APPLE P/N 353S3069

R6402 = HIGH = 400 KHZ
SPEAKER AMP GAIN = +15.2 DB
SPEAKER AMP RIN = 104K NOMINAL W/ +15.2 DB GAIN
FC_HPF, TWEETERS = ~850 HZ (0.0018 UF)
FC_HPF, WOOFERS = ~22.5 HZ (0.068 UF)



SYNC_MASTER=K60_DAVID SYNC_DATE=01/06/2011

PAGE TITLE: AUDIO: SPEAKER AMP_1

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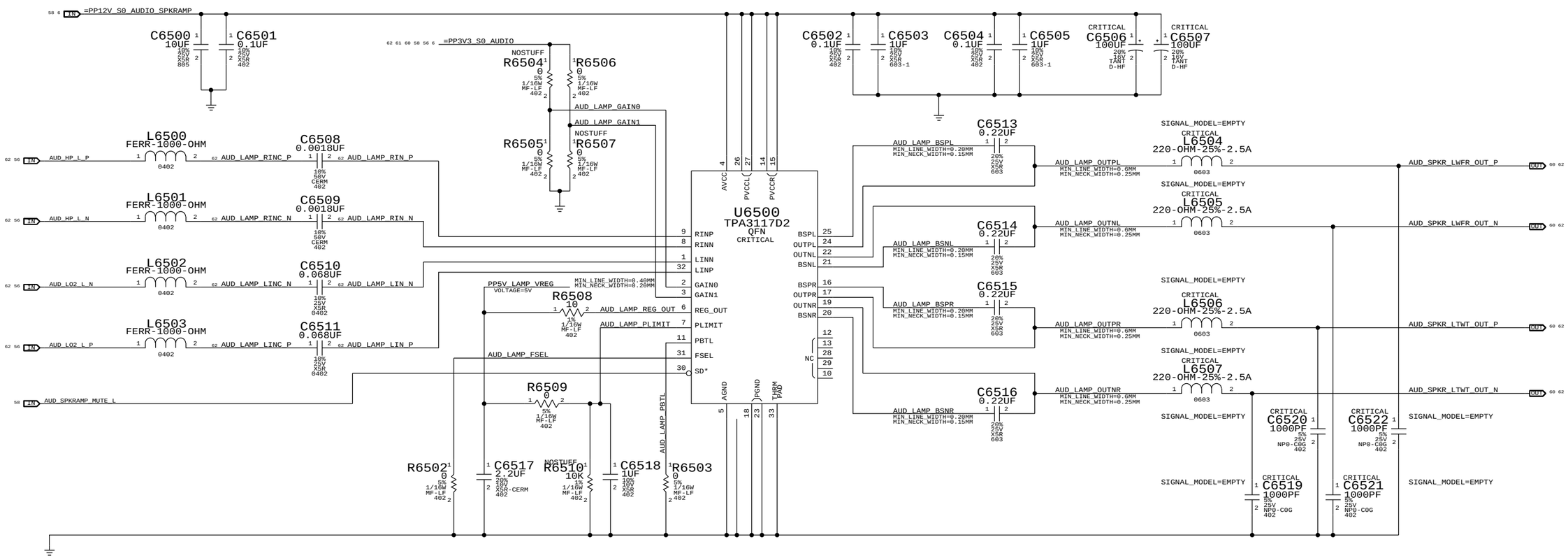
LEFT CH SPEAKER AMP
APPLE P/N 353S3069

R6502 = LOW = 300 KHZ
SPEAKER AMP GAIN = +15.2 DB
SPEAKER AMP RIN = 104K NOMINAL W/ +15.2 DB GAIN
FC_HPF, TWEETERS = ~850 HZ (0.0018 UF)
FC_HPF, WOOFERS = ~22.5 HZ (0.068 UF)



SYNC_MASTER=K60_DAVID SYNC_DATE=01/06/2011

PAGE TITLE
AUDIO: SPEAKER AMP

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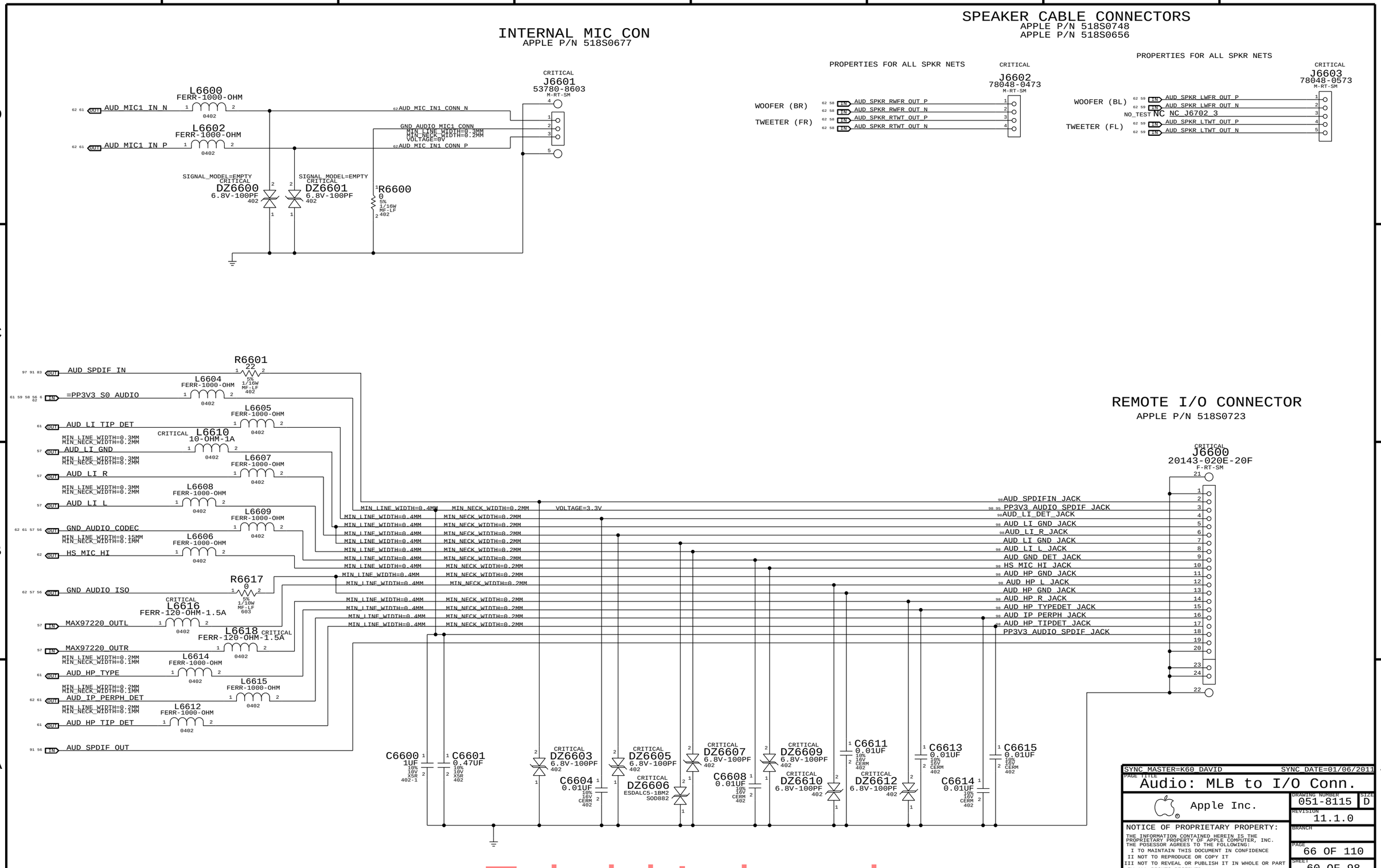

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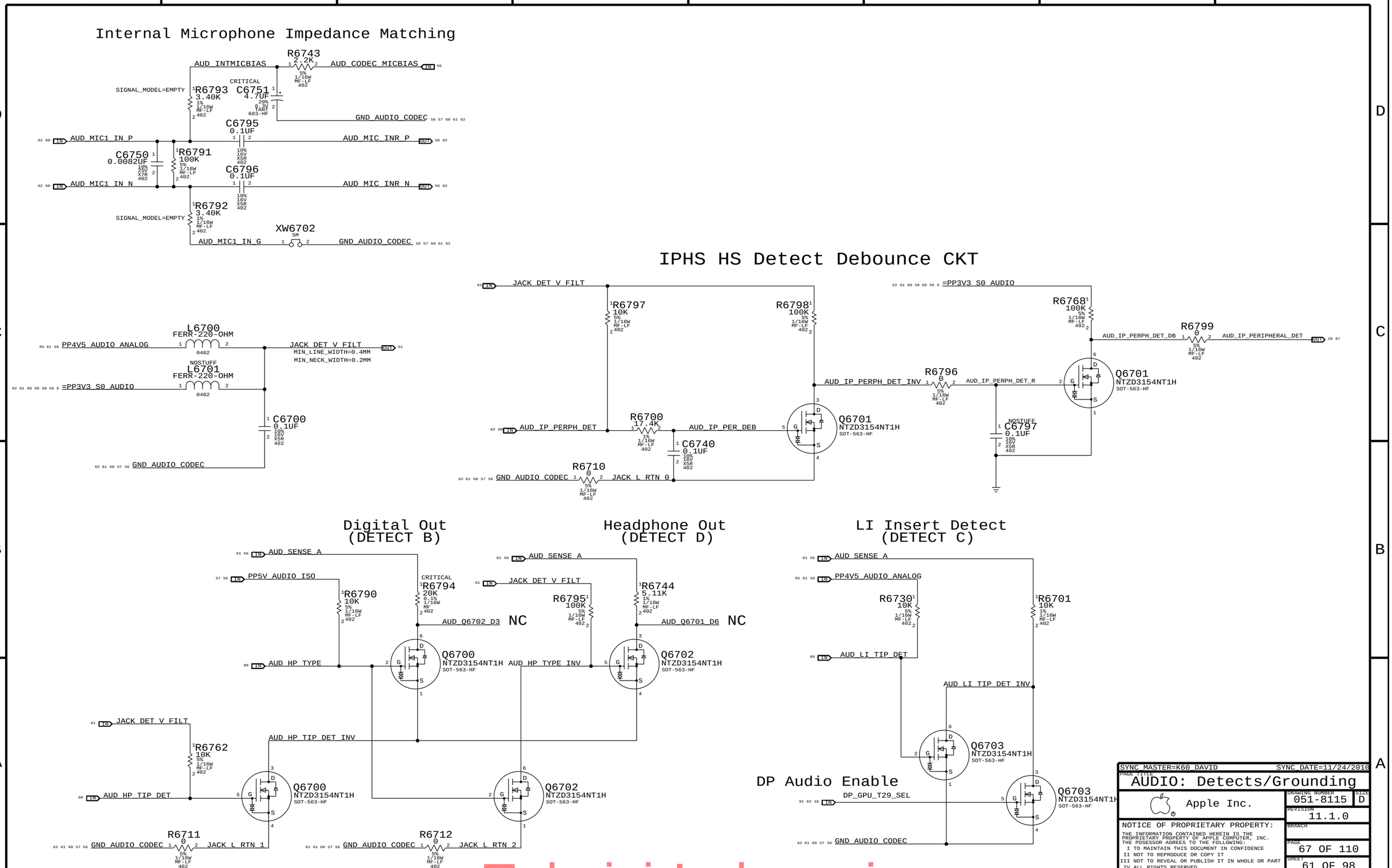

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	0X0A (D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X02 (2)	0X02 (2)	0X09 (09)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	0X0D (B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
LINE IN	0X05 (5)	0X12 (12,C)	N/A	0X12 (C)
SPDIF IN	0X07 (7)	0x0F (15)	N/A	N/A
INTERNAL MIC	0X06 (6)	0X0E (14,LEFT & RIGHT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	COUGAR POINT GPIO 16	COUGAR POINT GPIO 5 (RCVR INT) COUGAR POINT GPIO 3 (PERIPH DET)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0.1 MM	?
SPKROUT	*	0.2 MM	?

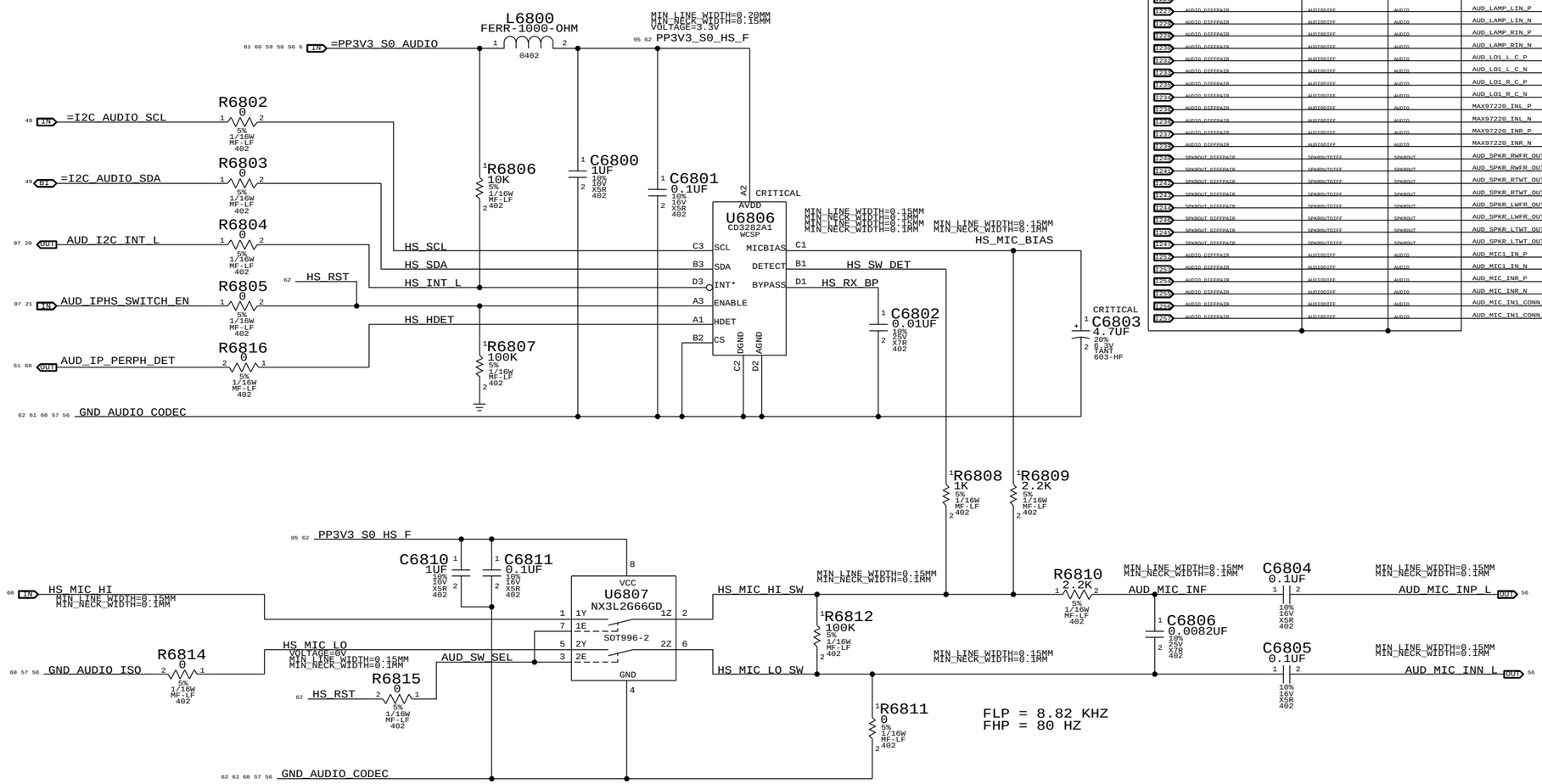
NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
U6806 B1	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HP_L_P	56 59
U6806 B2	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HP_L_N	56 59
U6806 B3	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HP_R_P	56 58
U6806 B4	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HP_R_N	56 58
U6806 B7	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	56 57
U6806 B8	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_N	56 57
U6806 B9	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	56 57
U6806 B10	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_N	56 57
U6806 B11	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	56 59
U6806 B12	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	56 59
U6806 B13	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	56 58
U6806 B14	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	56 58
U6806 B17	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_P	58
U6806 B18	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_N	58
U6806 B19	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_P	58
U6806 B20	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_N	58
U6806 B21	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_P	58
U6806 B22	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_N	58
U6806 B23	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_P	58
U6806 B24	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_N	58
U6806 B25	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_P	59
U6806 B26	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_N	59
U6806 B27	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_P	59
U6806 B28	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_N	59
U6806 B29	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_P	59
U6806 B30	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_N	59
U6806 B31	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_P	59
U6806 B32	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_N	59
U6806 B33	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_P	57
U6806 B34	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_N	57
U6806 B35	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_P	57
U6806 B36	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_N	57
U6806 B37	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_P	57
U6806 B38	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_N	57
U6806 B39	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_P	57
U6806 B40	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_N	57
U6806 B41	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_P	58 60
U6806 B42	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_N	58 60
U6806 B43	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_P	58 60
U6806 B44	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_N	58 60
U6806 B45	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_P	59 60
U6806 B46	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_N	59 60
U6806 B50	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_P	59 60
U6806 B47	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_N	59 60
U6806 B48	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC1_IN_P	60 61
U6806 B49	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC1_IN_N	60 61
U6806 B51	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INR_P	56 61
U6806 B52	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INR_N	56 61
U6806 B53	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_IN1_CONN_P	60
U6806 B54	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_IN1_CONN_N	60

MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2640



SYNC_MASTER=K60_DAVID SYNC_DATE=01/06/2011

PAGE TITLE
AUDIO: Mikey

Apple Inc.

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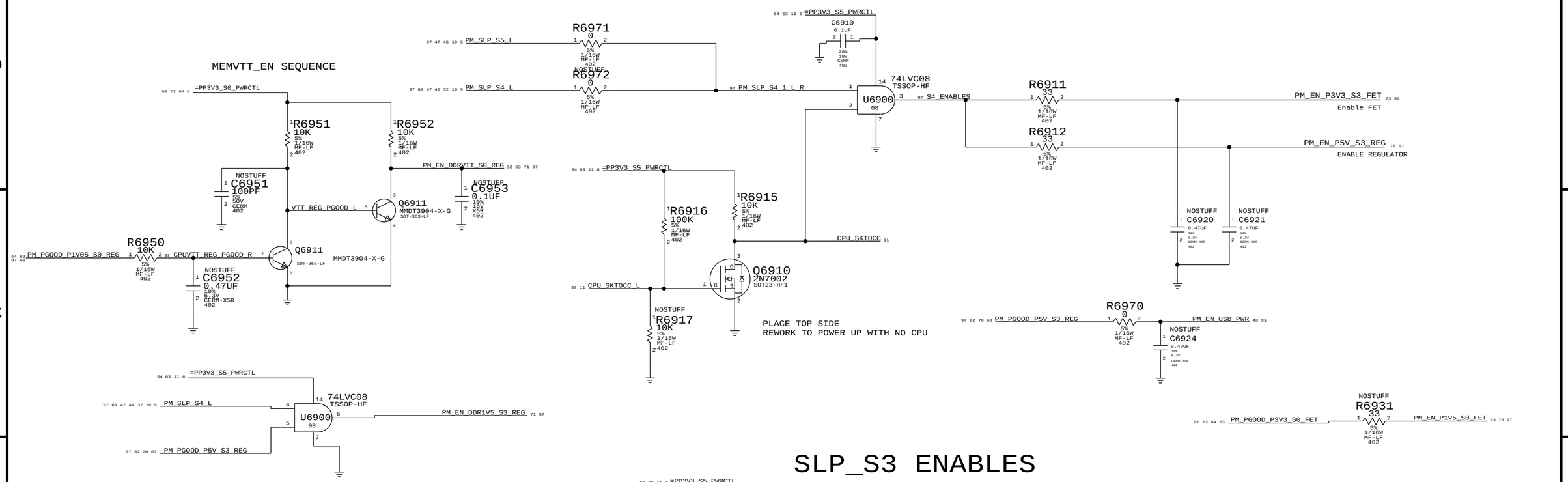
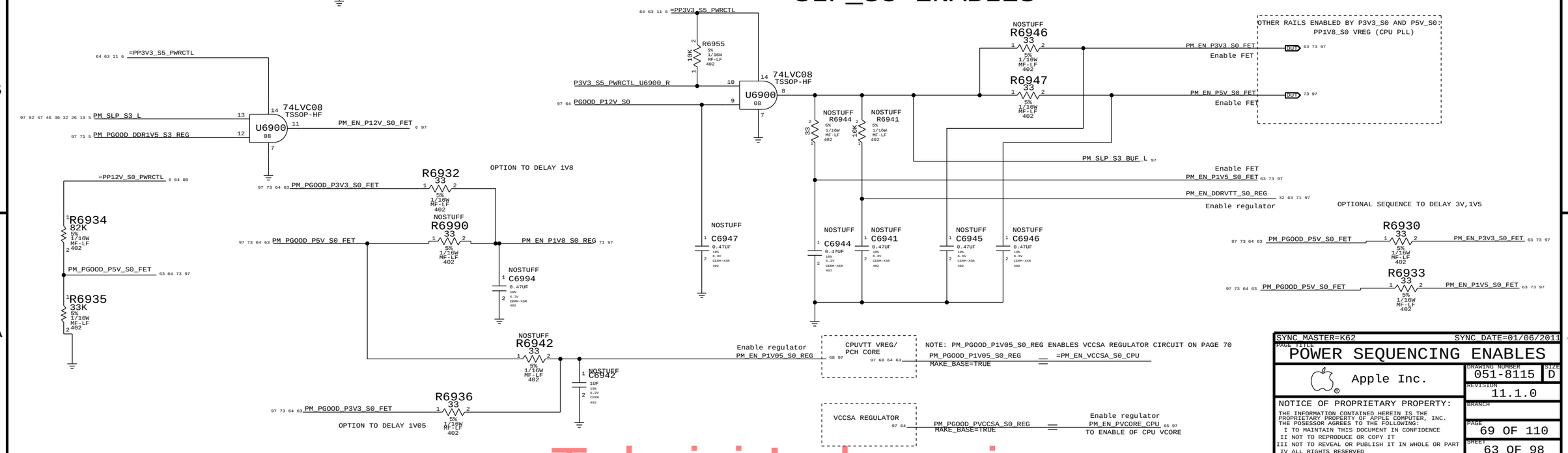
SLP_S4 ENABLES



SLP_S3 ENABLES



SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
POWER SEQUENCING ENABLES

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

REVISION 11.1.0

BRANCH

PAGE 69 OF 110

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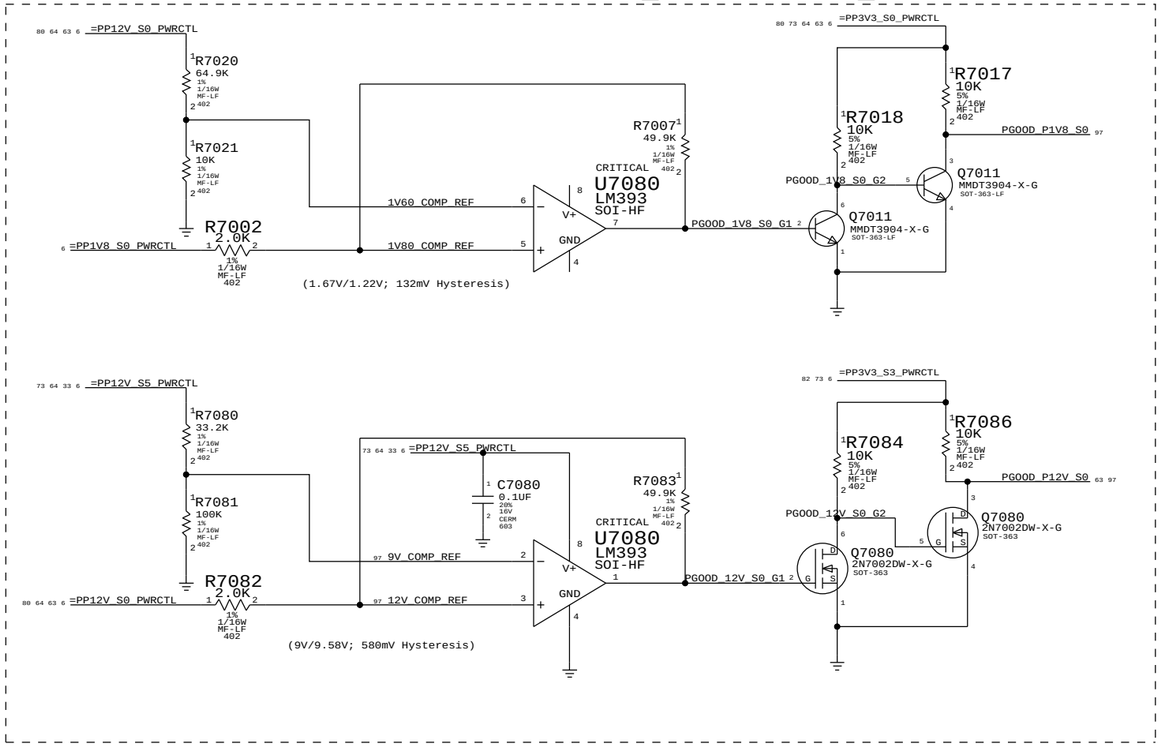
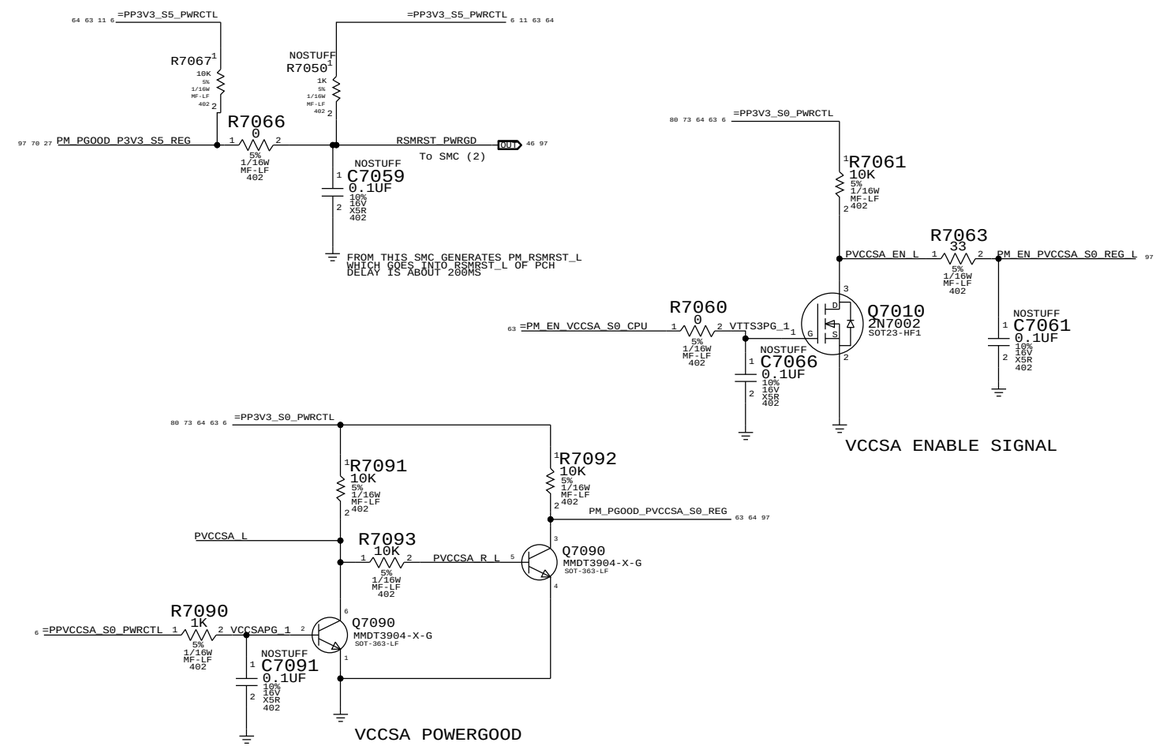
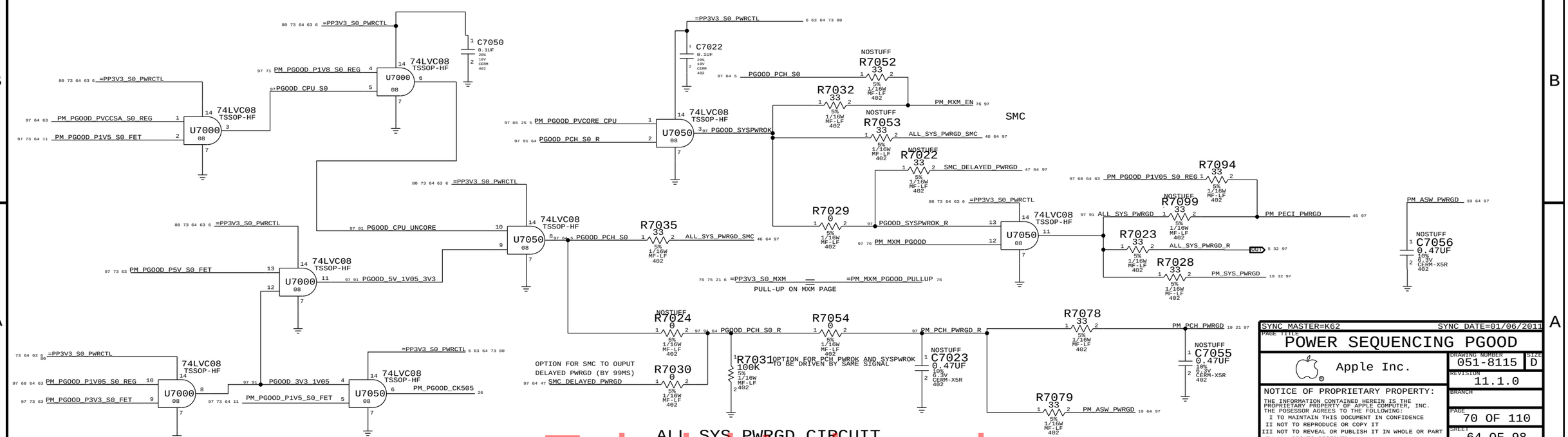
PGOOD COMPARATORS FOR PP1V8_S0 AND PP12V_S0



S0 RAILS PGOOD





ALL_SYS_PWRGD CIRCUIT

SYNC_MASTER=K62	SYNC_DATE=01/06/2011
PAGE TITLE	POWER SEQUENCING PGOOD
Apple Inc.	DRAWING NUMBER 051-8115
	SIZE D
	REVISION 11.1.0
	BRANCH
	PAGE 70 OF 110
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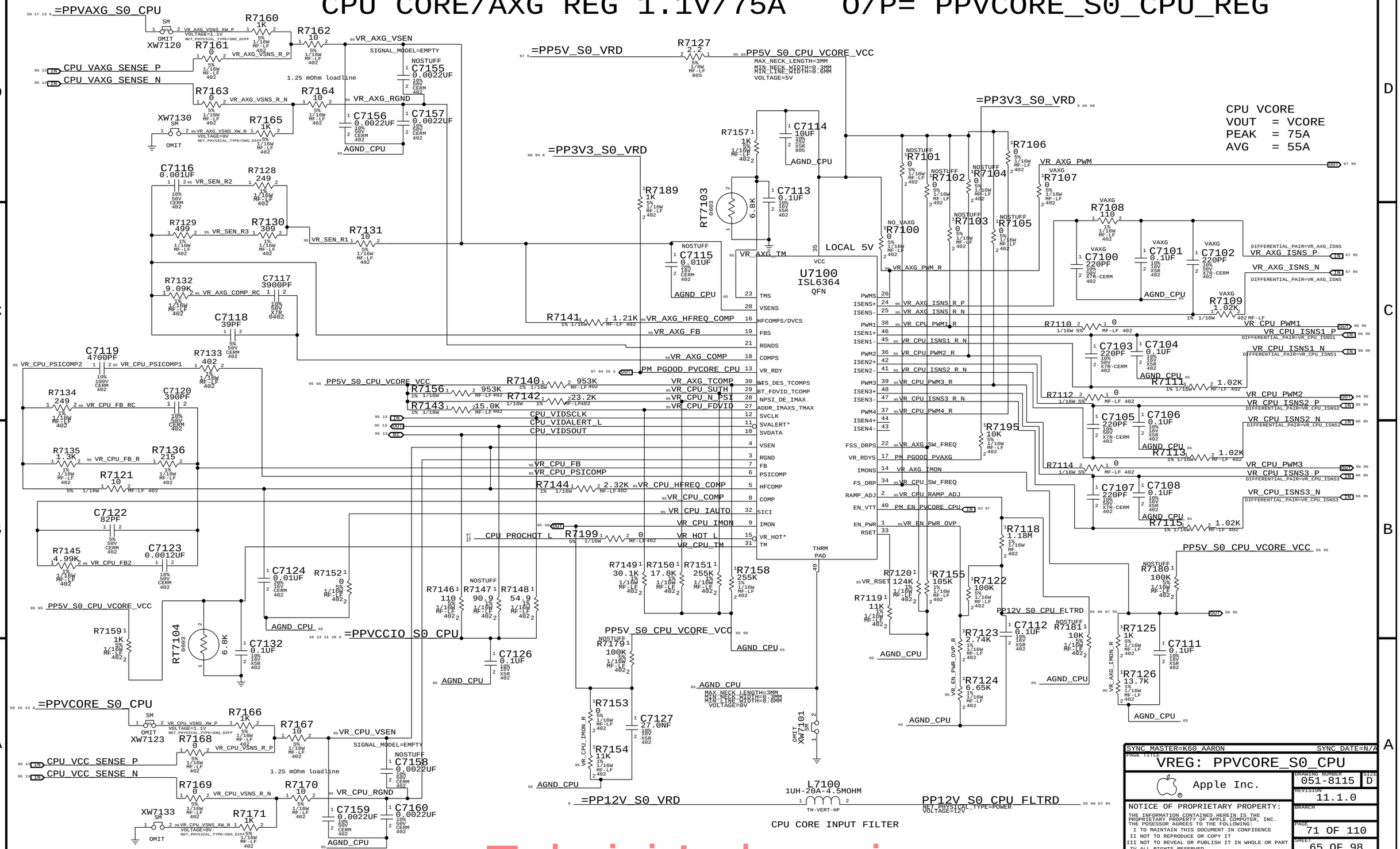
CPU CORE/AXG REG 1.1V/75A O/P= PPVCORE_S0_CPU_REG



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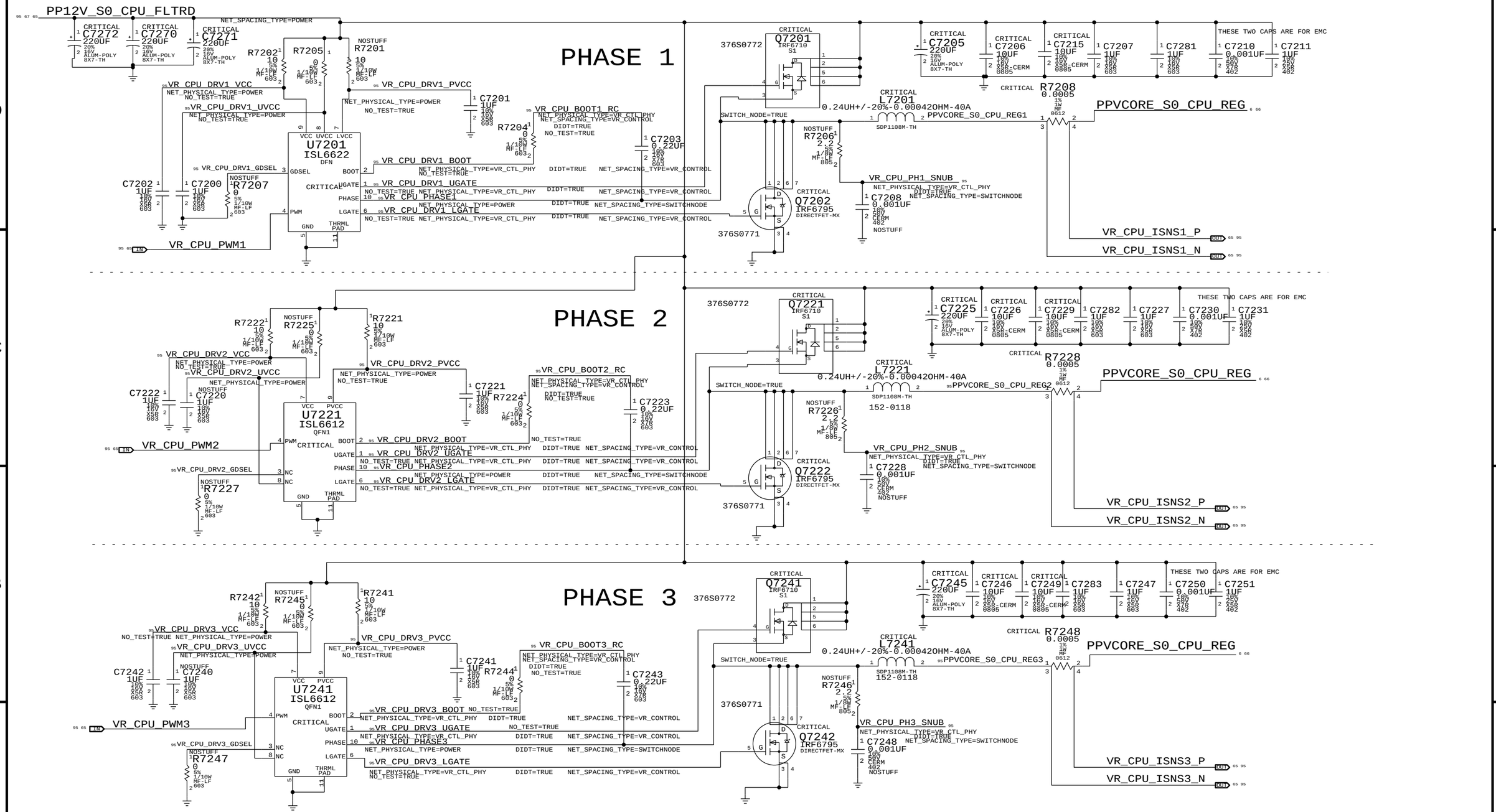

SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE
VREG: CPU CORE - PHASES 1-3

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

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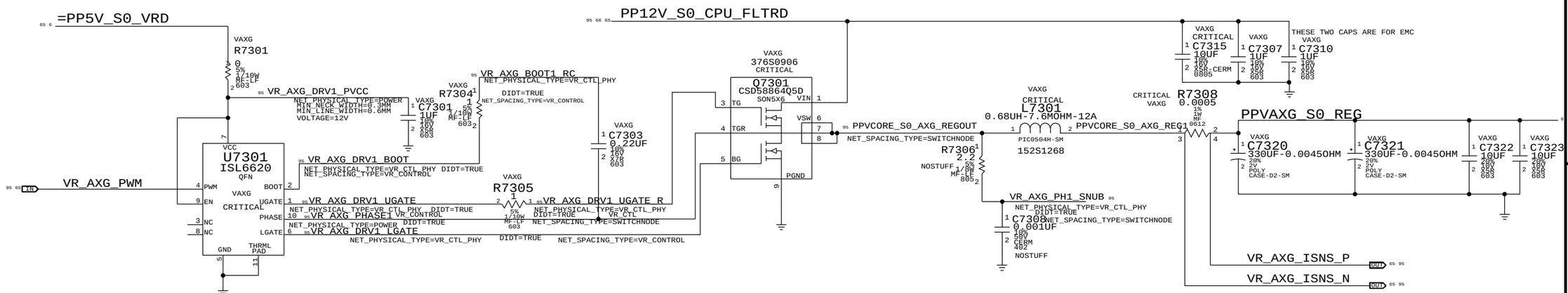
AXG PHASE (MAX 15A)



SYNC_MASTER=K60_AARON SYNC_DATE=N/A

PAGE TITLE
VREG:AXG PHASE/CORE - CAPS

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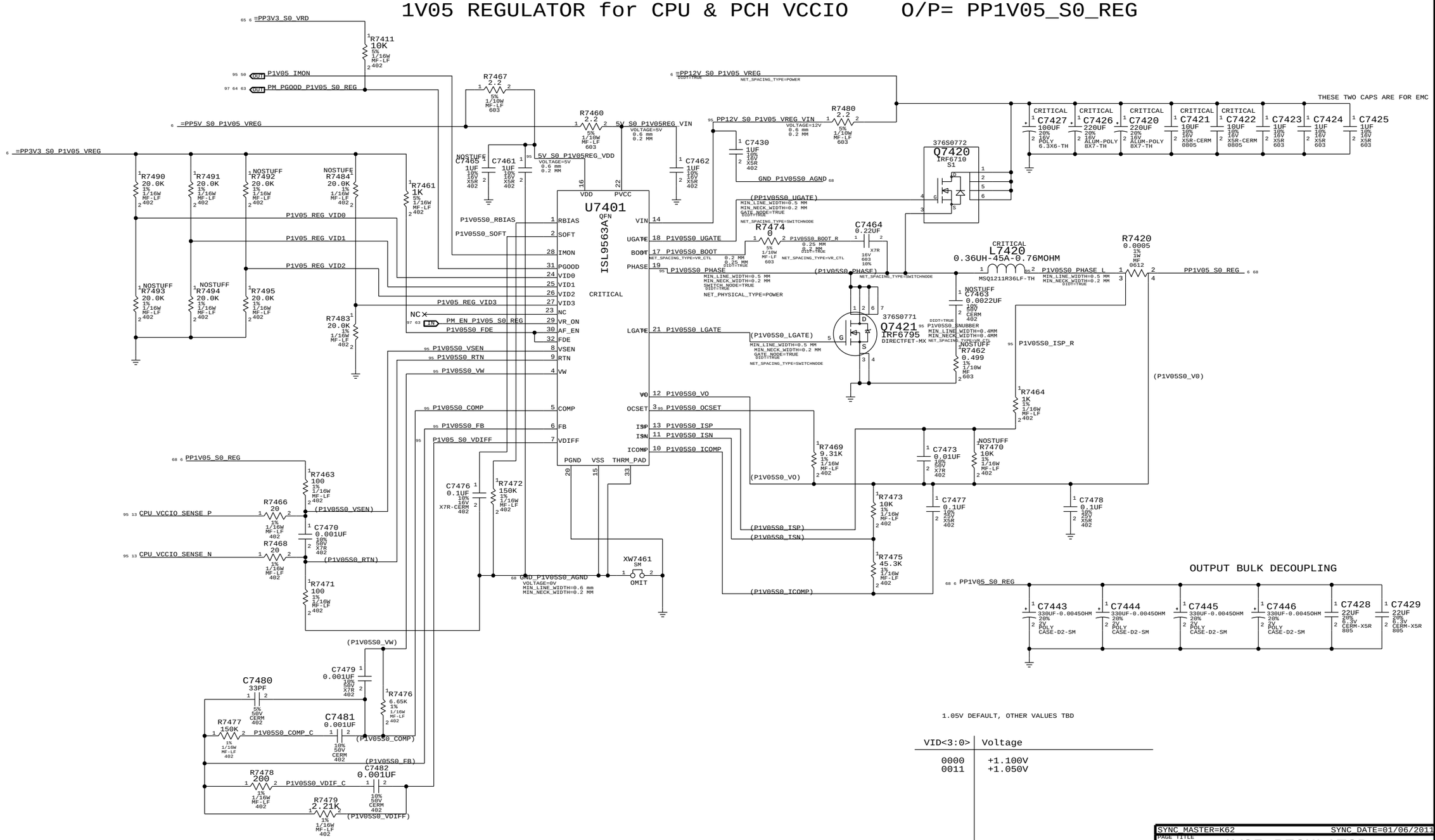
1V05 REGULATOR for CPU & PCH VCCIO O/P= PP1V05_S0_REG



1.05V DEFAULT, OTHER VALUES TBD

VID<3:0>	Voltage
0000	+1.100V
0011	+1.050V

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: 1V05 REGULATOR

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DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

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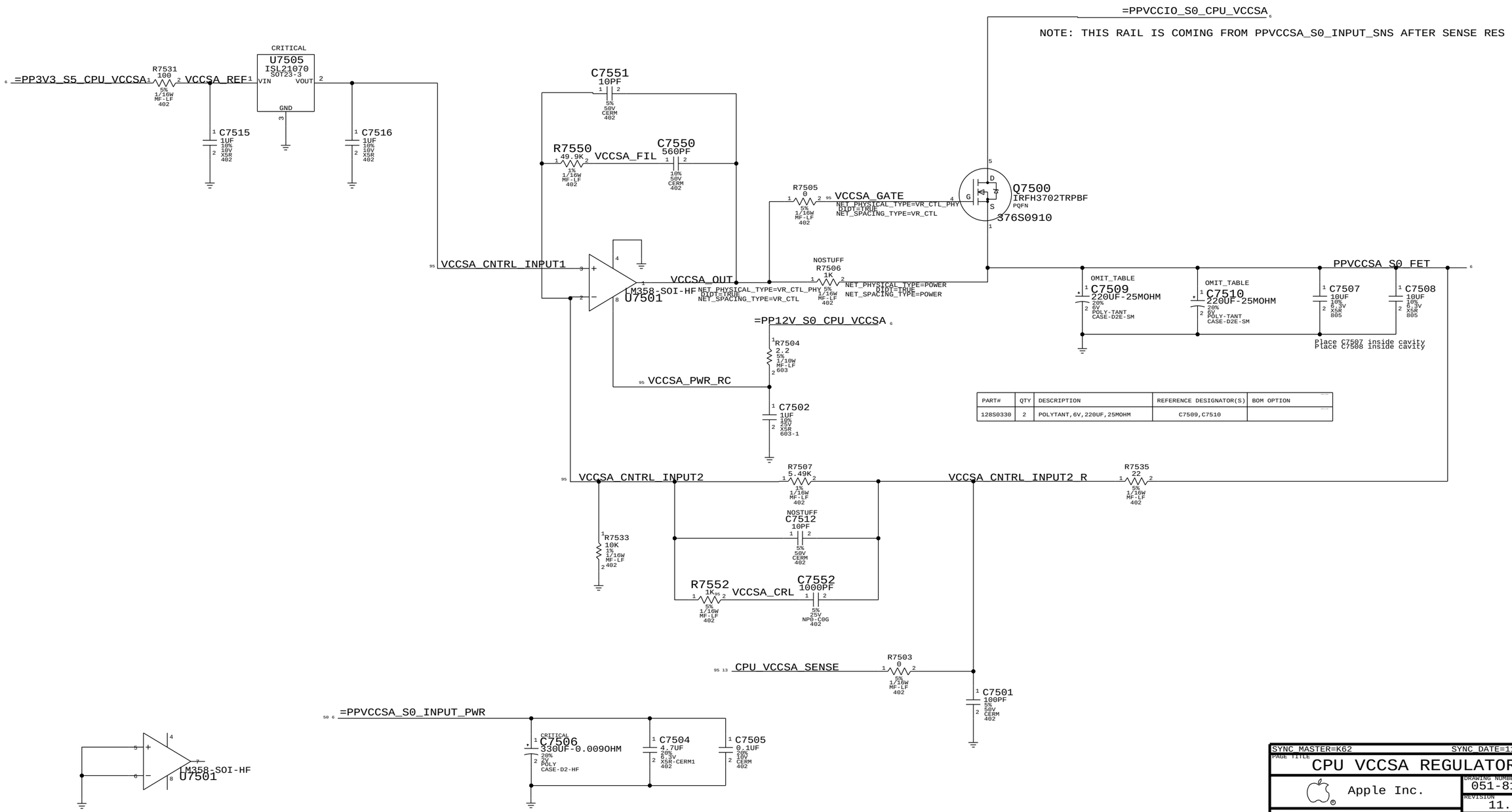
CPU VCCSA 0.925V (8.8A MAX)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0330	2	POLYTANT,6V,220UF,25MOHM	C7509,C7510	

SYNC MASTER=K62 SYNC DATE=11/15/2010

PAGE TITLE
CPU VCCSA REGULATOR

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DRAWING NUMBER 051-8115 SIZE D

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3V3 S5 REGULATOR

5V S3 REGULATOR

Power Rating ?

3V3 OUTPUT

5V OUTPUT

=PP12V_S5_P5VS3_VREG

NET_SPACING_TYPE=POWER

EMC CAPS
PLACE CLOSE TO FET

C7718 100UF 20% 16V POLY 6.3X6-TH
C7712 10UF 10% 16V X5R-CERM 0805
C7710 10UF 10% 16V X5R-CERM 0805
C7711 1UF 10% 16V X5R 603
C7722 1UF 10% 16V X5R 603

NET_PHYSICAL_TYPE=POWER

C7719 100UF 20% 16V POLY 6.3X6-TH
C7766 100UF 20% 16V POLY 6.3X6-TH
C7767 100UF 20% 16V POLY 6.3X6-TH
C7768 100UF 20% 16V POLY 6.3X6-TH
C7758 10UF 10% 16V X5R-CERM 0805
C7765 10UF 10% 16V X5R-CERM 0805

=PP3V3_S5_VRD

R7726 20K 5% 1/16W MF-LF 402

=PP12V_S5_P5VS3_VREG

NOSTUFF
R7725 20K 5% 1/16W MF-LF 402

PP5V_S5_LDO

EMC: C7754,C7755
PLACE AT Q7330

C7754 1UF 10% 16V X5R 603
C7755 1UF 10% 16V X5R 603

PP3V3_S5_REG

R7776 0.002 1% 1/4W MF-LF 1206

CRITICAL
L7710 2.2UH-14A MMD06CZ-SM

PP3V3_S5_REG_R
NET_PHYSICAL_TYPE=POWER

C7790 0.01UF 10% 16V CERM 402
R7790 15.8K 1% 1/10W MF-LF 402

R7791 15.8K 1% 1/16W MF-LF 402

Q7710
RJK0384DPA
WPAK
376S0801

D1
G1
S1/D2
G2
S2

1 (P3V3S5_UGATE)
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
GATE_NODE=TRUE
NET_SPACING_TYPE=VR_CONTROL

6 (P3V3S5_LGATE)
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
GATE_NODE=TRUE
NET_SPACING_TYPE=VR_CONTROL

NET_PHYSICAL_TYPE=POWER

C7730 1000PF 5% 25V NP0-C0G 402
NOSTUFF

NET_SPACING_TYPE=VR_CTL
NOSTUFF
R7730 0.499 1% 1/10W MF 603

P3V3S5_REG_SNUB

C7714 0.1UF 10% 50V X7R 603-1

P3V3S5_REG_BOOT_R
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
NET_SPACING_TYPE=VR_CONTROL
(P3V3S5_PHASE)

R7710 0 5% 1/10W MF-LF 603

NET_SPACING_TYPE=VR_CONTROL
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM

MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
NET_SPACING_TYPE=SWITCHNODE
NET_PHYSICAL_TYPE=POWER

OUTPUT BULK DECOUPLING:

C7715 10UF 10% 16V X5R-CERM 0805
C7717 10UF 10% 16V X5R-CERM 0805
C7721 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

128S0237
CRITICAL

PLACEMENT_NOTE=PLACE NEXT TO C7716
XW7716
SM
OMIT

R7720 45.3K 1% 1/16W MF-LF 402
<Ra>

R7721 10.0K 0.5% 1/16W MF 402
<Rb>

R7724 976 1% 1/16W MF-LF 402
P3V3S5_REG_FB_R

C7720 1000PF 5% 25V NP0-C0G 402

C7723 0.1UF 20% 16V CERM 603
C7716 0.1UF 20% 16V CERM 603

EMC CAPS
PLACE CLOSE TO L

Vout = 0.6V * (1 + Ra / Rb)

PM_PGOOD_P3V3_S5_REG
P3V3S5_REG_UGATE
P3V3S5_REG_BOOT
P3V3S5_REG_PHASE
P3V3S5_REG_LGATE
P3V3S5_REG_ISEN
P3V3S5_REG_OCSET
P3V3S5_REG_VOUT1
P3V3S5_REG_FB
PM_EN_P3V3_S5_REG

R7722 68K 5% 1/16W MF-LF 402

R7723 33K 5% 1/16W MF-LF 402

U7700
ISL62383
QFN
CRITICAL

LDO5 VCC1 VCC2 VIN_5V_S5_REG_RC
VIN 17
FCCM 3 TP_P5VS3_REG_FCCM
PGOOD1 7 PGOOD2 1
UGATE1 14 UGATE2 22 P5VS3_REG_UGATE
BOOT1 15 BOOT2 21 P5VS3_REG_BOOT
PHASE1 13 PHASE2 23 P5VS3_REG_PHASE
LGATE1 16 LGATE2 20 P5VS3_REG_LGATE
ISEN1 10 ISEN2 26 P5VS3_REG_ISEN
OCSET1 11 OCSET2 25 P5VS3_REG_OCSET
VOUT1 9 VOUT2 27 P5VS3_REG_VOUT2
FB1 8 FB2 28 P5VS3_REG_FB
FSET1 6 FSET2 2 P5VS3_REG_FSET2
EN1 12 EN2 24
THRM PAD 33 PGND 33

P3V3S5_REG_FSET1
C7701 0.01UF 10% 16V CERM 402
R7701 16.5K 1% 1/16W MF-LF 402

C7742 4.7UF 20% 6.3V CERM 603

NET_PHYSICAL_TYPE=POWER
R7740 2.2 5% 1/8W MF-LF 805

P5V_S5_LDO_R

R7741 1 5% 1/8W MF-LF 805

P5V_S5_VCC1
C7740 1UF 10% 16V X5R 603
C7741 1UF 10% 16V X5R 603
C7743 1UF 10% 16V X5R 603

PM_PGOOD_P5V_S3_REG OUT

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=VR_CONTROL

CRITICAL
Q7750
FDMS0346
POWER56
376S0875

R7750 0 5% 1/10W MF-LF 603

P5V3S5_REG_BOOT_R
MIN_NECK_WIDTH=0.2 MM
MIN_LINE_WIDTH=0.6MM
NET_SPACING_TYPE=VR_CONTROL

C7756 0.1UF 10% 25V X5R 402

NET_SPACING_TYPE=SWITCHNODE
NET_PHYSICAL_TYPE=POWER

NOSTUFF
C7757 0.001UF 10% 50V CERM 402

5V_SNUBBER
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=SWITCHNODE
R7752 0.499 1% 1/10W MF 603
NOSTUFF

CRITICAL
Q7751
FDMS0355S
POWER56
376S0917

EMC: C7763,C7764
PLACE AT L7750.2

C7763 0.001UF 10% 50V X7R 402
C7764 0.001UF 10% 50V X7R 402

PP5V_S3_REG

R7775 0.002 1% 1/4W MF-LF 1206

CRITICAL
L7750
2.2UH+/-20%-0.0069OHM-16A
PIC1005H-SM

PP5V_S3_REG_R
NET_PHYSICAL_TYPE=POWER

R7770 9.76K 1% 1/16W MF-LF 402
C7770 27.0NF 10% 16V X5R 402

R7771 9.76K 1% 1/16W MF-LF 402

OUTPUT BULK DECOUPLING:

C7760 10UF 20% 6.3V CERM 805-1
C7769 10UF 20% 6.3V CERM 805-1
C7761 330UF 20% 6.3V POLY-TANT CASE-D3L-SM
C7762 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

XW7751
SM
OMIT

PM_EN_P5V_S3_REG

C7747 0.01UF 10% 16V CERM 402
R7747 16.5K 1% 1/16W MF-LF 402

NOSTUFF
C7777 0.001UF 10% 50V CERM 402

R7759 976 1% 1/16W MF-LF 402
P5VS5_REG_FB_R

C7759 1000PF 5% 25V NP0-C0G 402

R7755 75K 1% 1/16W MF-LF 402
RA

RB
R7756 10K 1% 1/16W MF-LF 402

SYNC_MASTER=K62	SYNC_DATE=01/06/2011
PAGE TITLE: 5V_S3 / 3V3_S5 VREGS	
Apple Inc.	DRAWING NUMBER: 051-8115 SIZE: D
	REVISION: 11.1.0
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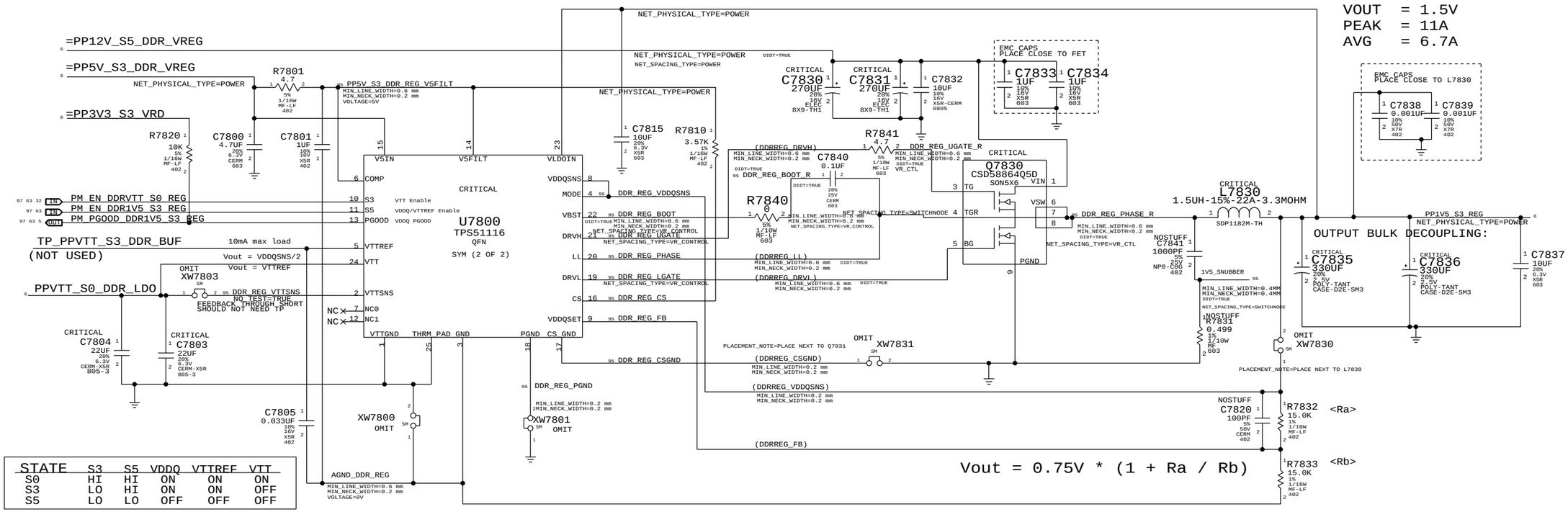
1.5 V DDR SUPPLY

PPDDR_S3_REG
VOUT = 1.5V
PEAK = 11A
AVG = 6.7A



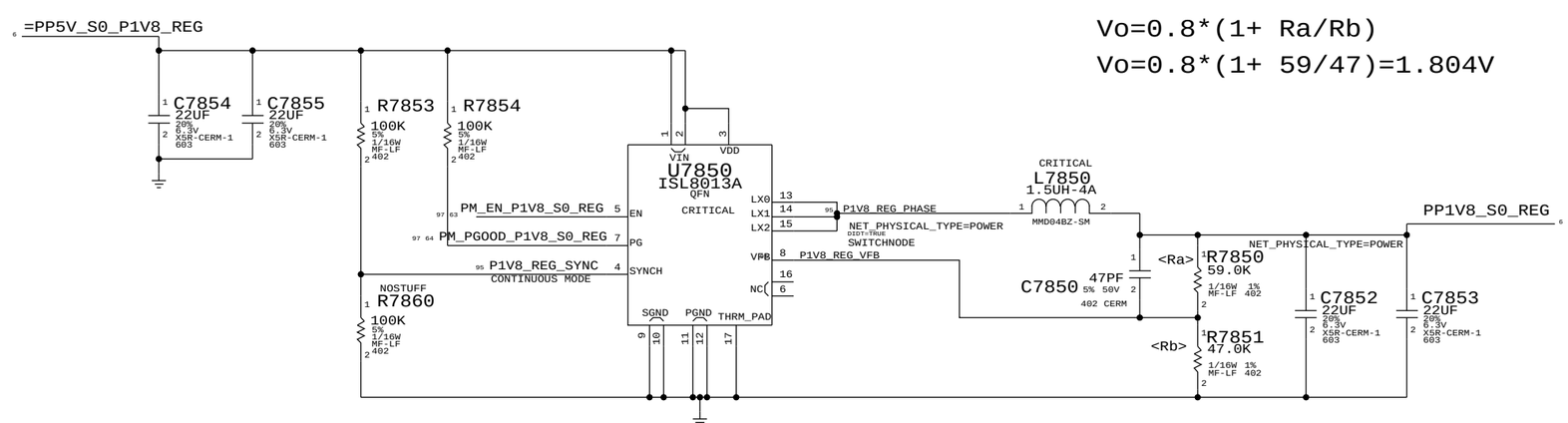
STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF
S5	LO	LO	OFF	OFF	OFF

Vout = 0.75V * (1 + Ra / Rb)

1.8 V SUPPLY

1A Average current

Vo=0.8*(1+ Ra/Rb)
Vo=0.8*(1+ 59/47)=1.804V



SYNC MASTER=K62	SYNC DATE=01/06/2011
PAGE TITLE	1.5V / 1.8V VREGS
Apple Inc.	DRAWING NUMBER 051-8115 SIZE D
	REVISION 11.1.0
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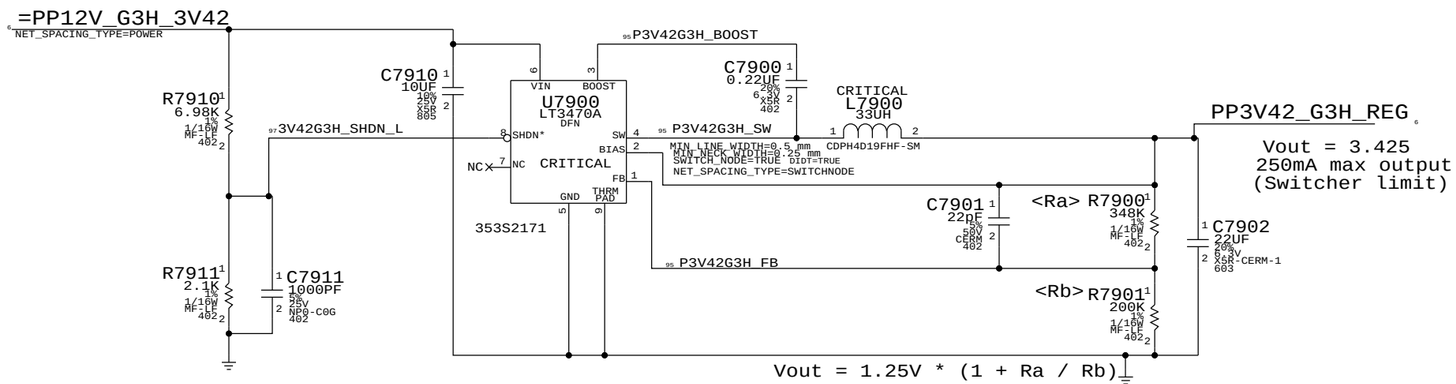
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE: 3.42 G3HOT SUPPLY

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

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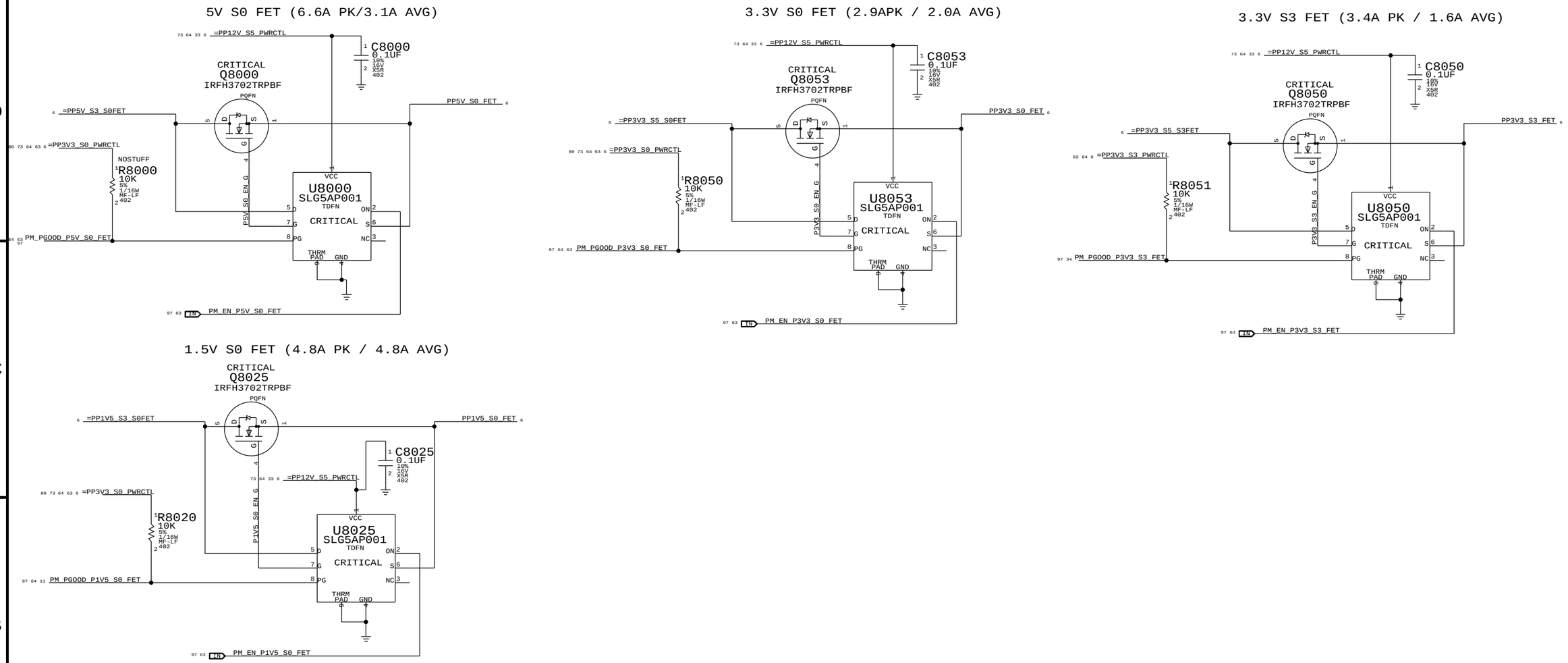

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
S3+S0 FETS

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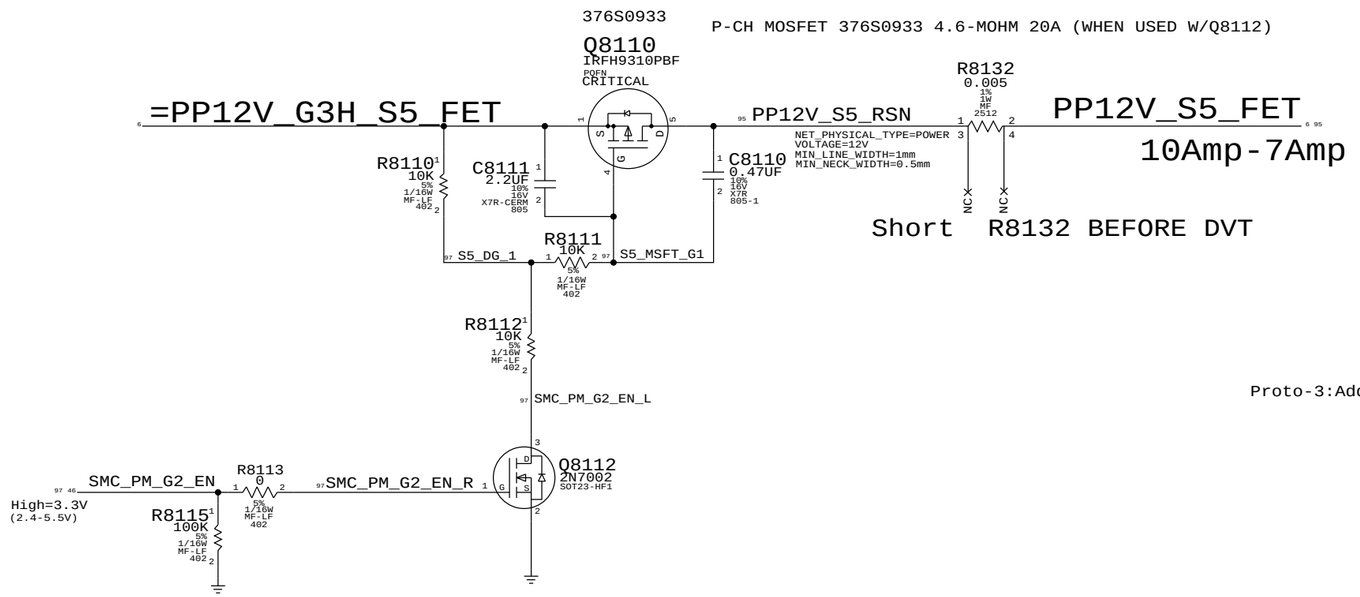

SYNC MASTER=K60 JERRY SYNC DATE=01/06/2011

PAGE TITLE
12V_S0 & 12V_S5 switch

Apple Inc.

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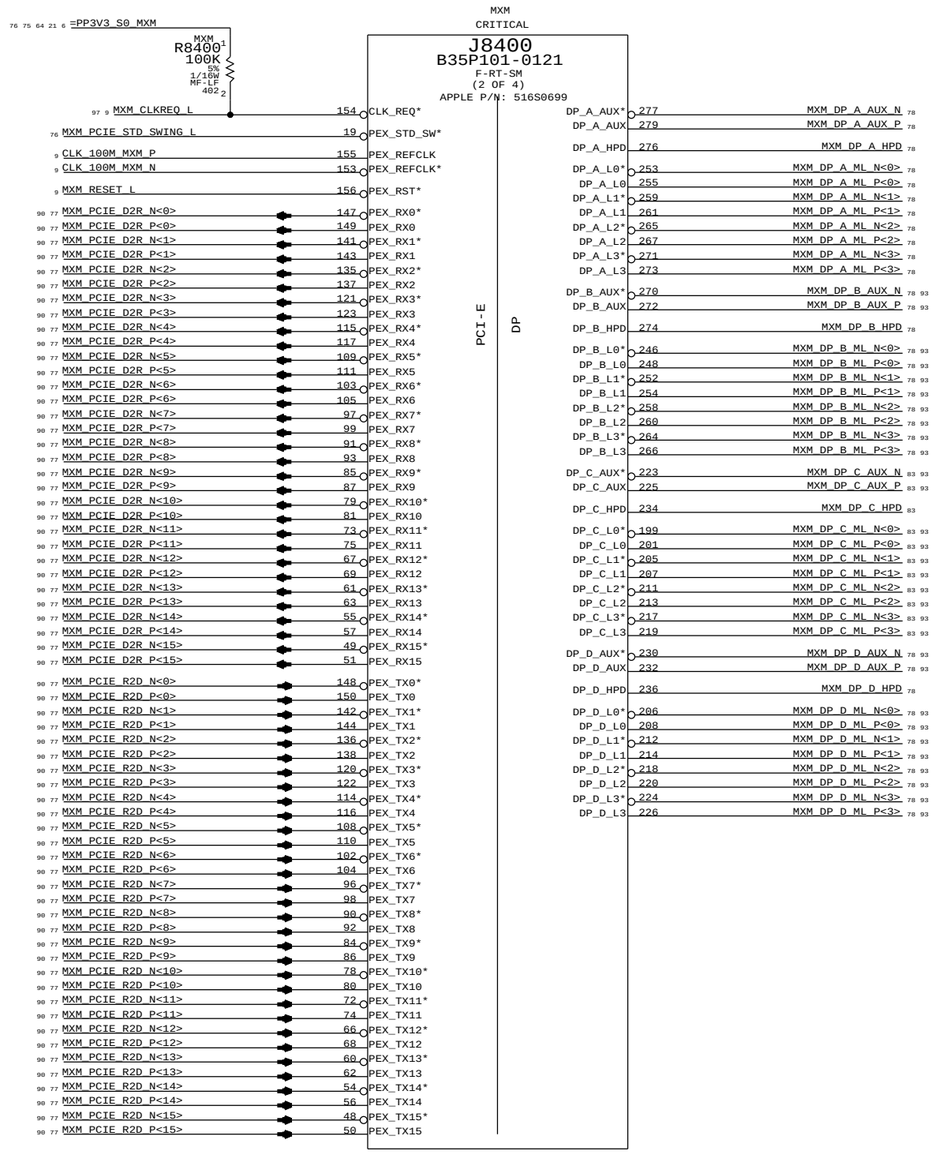
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- MXM



MXM SPEC POWER REQUIREMENTS

(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.0 A	3.3 W
5V	2.5 A	12.5 W
PWR (7-20V)	UP TO 10 A	PLATFORM DEPENDENT

MXM DP PORT ROUTING

	K62	K60
DP A	EXT DP1	EXT DP1
DP B	T29 DP2	T29 DP2
DP C	INT DP	INT DP
DP D	T29 DP1	T29 DP1
DP E	EXT DP2	

SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE
MXM PCIe, DP & Power

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

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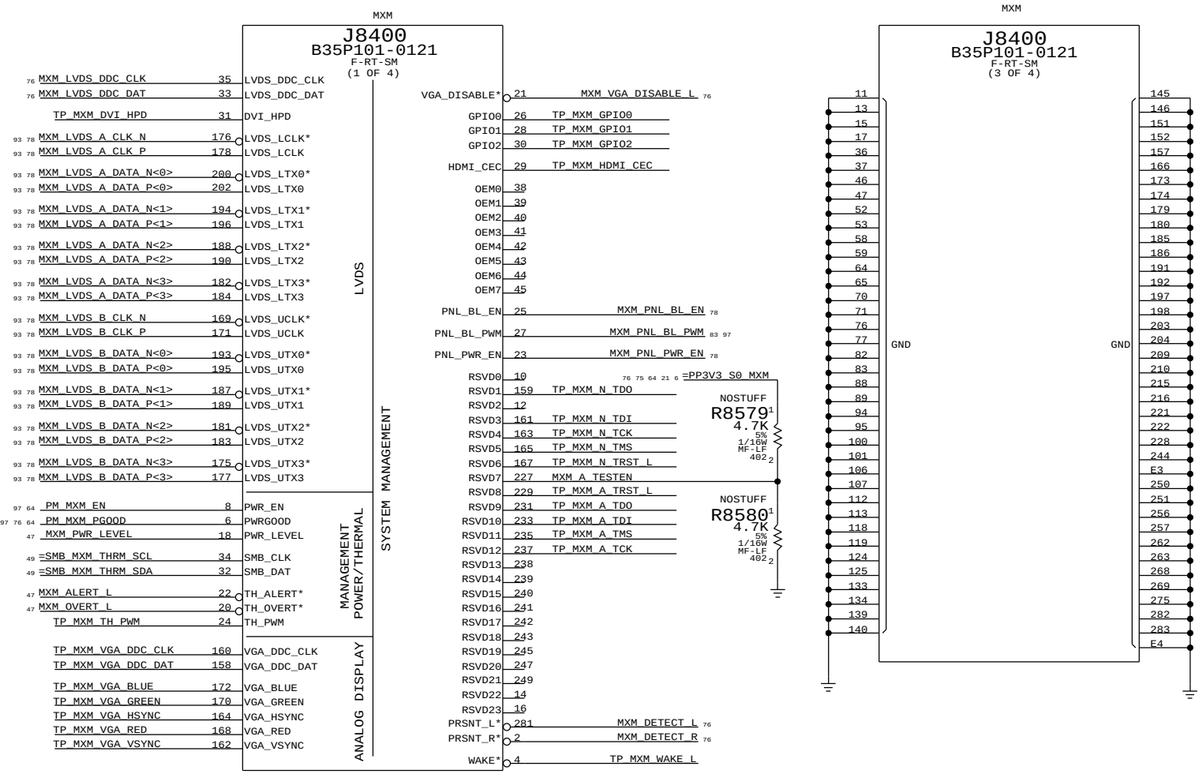
Page Notes

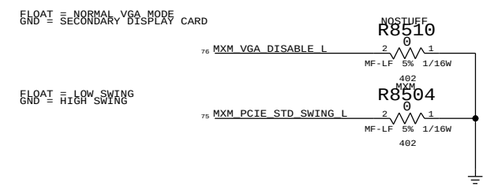
Power aliases required by this page:
- =PP3V3_S0_MXM

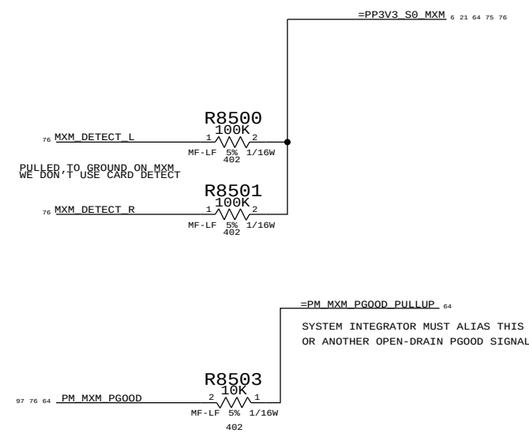
Signal aliases required by this page:
- =SMB_MXM_THRM_DATA - =PM_MXM_PGOOD_PULLUP
- =SMB_MXM_THRM_CLK

BOM options provided by this page:

PULLUPS & PULLDOWNS AT MXM CONNECTOR

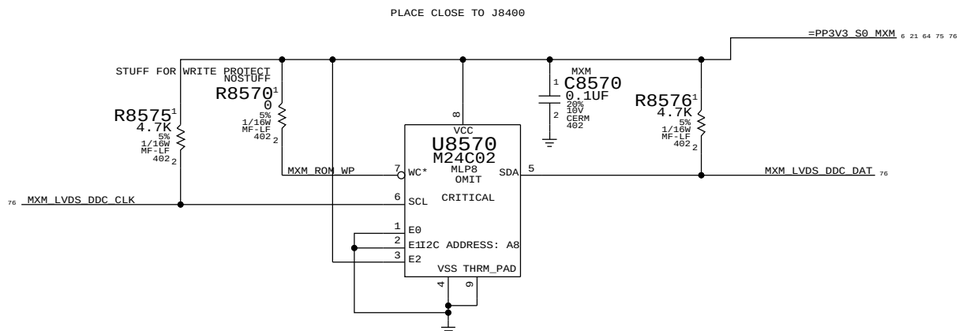






MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J8400



SYNC_MASTER=K60_MASTER	SYNC_DATE=N/A
PAGE TITLE: MXM I/O	
Apple Inc.	DRAWING NUMBER: 051-8115 SIZE: D
	REVISION: 11.1.0
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MXM TX CAPS

PEG_R2D_C_P<0>	MXM C8600	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<15>	
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MXM RX CAPS

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SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
MXM PCIE CAPS

Apple Inc.

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Page Notes

Power aliases required by this page:

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

MXM ALIAS

75	MXM_DP_A_ML_P<0..3>	DP_EXTA_ML_C_P<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE	84 93
75	MXM_DP_A_ML_N<0..3>	DP_EXTA_ML_C_N<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE	84 93
75	MXM_DP_A_AUX_P	DP_EXTA_AUXCH_C_P	MAKE_BASE=TRUE NO_TEST=TRUE	78 84 93
75	MXM_DP_A_AUX_N	DP_EXTA_AUXCH_C_N	MAKE_BASE=TRUE NO_TEST=TRUE	78 84 93
75	MXM_DP_A_HPD	DP_EXTA_HPD	MAKE_BASE=TRUE NO_TEST=TRUE	84

T29 CONN POWER CONTROL ALIAS

95 84	PP3V3_SW_DPAPWR	=PP3V3_SW_DPAPWR	6
97 36 33 19	PCIE_WAKE_L	=T29_WAKE_L	84

T29 MXM DP ALIAS

93 75	MXM_DP_D_ML_P<0..3>	DP_T29SNK0_ML_C_P<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE	86 96
93 75	MXM_DP_D_ML_N<0..3>	DP_T29SNK0_ML_C_N<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE	86 96
93 75	MXM_DP_D_AUX_P	DP_T29SNK0_AUXCH_C_P	MAKE_BASE=TRUE NO_TEST=TRUE	86 96
93 75	MXM_DP_D_AUX_N	DP_T29SNK0_AUXCH_C_N	MAKE_BASE=TRUE NO_TEST=TRUE	86 96
75	MXM_DP_D_HPD	DP_T29SNK0_HPD	MAKE_BASE=TRUE NO_TEST=TRUE	86
93 75	MXM_DP_B_ML_P<0..3>	DP_T29SNK1_ML_C_P<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE	86 96
93 75	MXM_DP_B_ML_N<0..3>	DP_T29SNK1_ML_C_N<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE	86 96
93 75	MXM_DP_B_AUX_P	DP_T29SNK1_AUXCH_C_P	MAKE_BASE=TRUE NO_TEST=TRUE	86 96
93 75	MXM_DP_B_AUX_N	DP_T29SNK1_AUXCH_C_N	MAKE_BASE=TRUE NO_TEST=TRUE	86 96
75	MXM_DP_B_HPD	DP_T29SNK1_HPD	MAKE_BASE=TRUE NO_TEST=TRUE	86

Unused MXM Interfaces

93 76	MXM_LVDS_A_CLK_N	NC_MXM_LVDS_A_CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE
93 76	MXM_LVDS_A_CLK_P	NC_MXM_LVDS_A_CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE
93 76	MXM_LVDS_A_DATA_N<3..0>	NC_MXM_LVDS_A_DATA_N<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
93 76	MXM_LVDS_A_DATA_P<3..0>	NC_MXM_LVDS_A_DATA_P<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
93 76	MXM_LVDS_B_CLK_N	NC_MXM_LVDS_B_CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE
93 76	MXM_LVDS_B_CLK_P	NC_MXM_LVDS_B_CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE
93 76	MXM_LVDS_B_DATA_N<3..0>	NC_MXM_LVDS_B_DATA_N<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
93 76	MXM_LVDS_B_DATA_P<3..0>	NC_MXM_LVDS_B_DATA_P<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE

Unused T29 Interfaces

96 86	T29_D2R_N<2..3>	NC_T29_D2R_N<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE		
96 86	T29_D2R_P<2..3>	NC_T29_D2R_P<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE		
96 86	T29_R2D_C_N<2..3>	NC_T29_R2D_C_N<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE		
96 86	T29_R2D_C_P<2..3>	NC_T29_R2D_C_P<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE		
86	T29_LSEO<3>	T29_LSEO_LSOE3	MAKE_BASE=TRUE NO_TEST=TRUE	T29_LSOE<3>	86
86	T29_LSEO<2>	T29_LSEO_LSEO2	MAKE_BASE=TRUE NO_TEST=TRUE	T29_LSOE<2>	86

UNUSED MXM CONTROL SIGNALS

76	MXM_PNL_BL_EN	NC_MXM_PNL_BL_EN	MAKE_BASE=TRUE NO_TEST=TRUE
76	MXM_PNL_PWR_EN	NC_MXM_PNL_PWR_EN	MAKE_BASE=TRUE NO_TEST=TRUE

DDC/AUX ALIAS

93 84 78	DP_EXTA_AUXCH_C_P	DP_EXTA_DDC_CLK	MAKE_BASE=TRUE	84
93 84 78	DP_EXTA_AUXCH_C_N	DP_EXTA_DDC_DATA	MAKE_BASE=TRUE	84

SYNC_MASTER=K60_AARON SYNC_DATE=07/18/2010

PAGE TITLE
DP ALIAS AND CONTROL

Apple Inc.

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System RTC Power Source & 32kHz / 25MHz Clock Generator

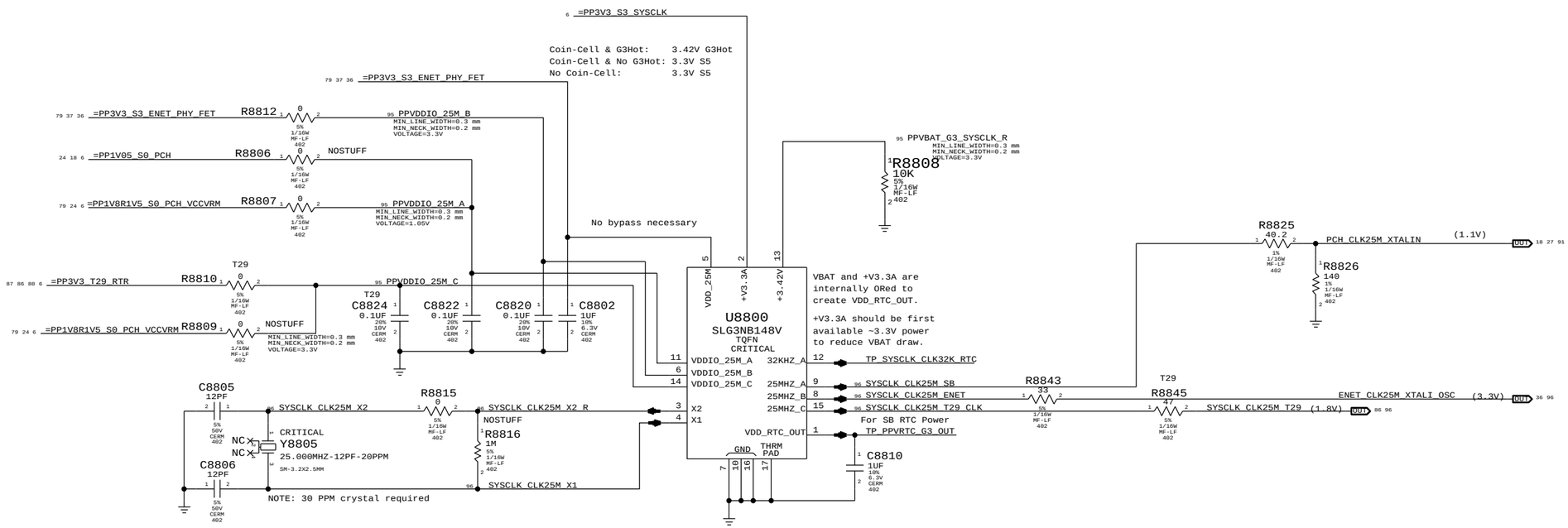
GreenCLK Implementation Notes:

VBAT: Alias as appropriate (see note below & Desktop Example)
+V3.3A: Alias as appropriate (see note below)
VDD_25M: 3.3V matching 'highest' VDDIO power state (ENET)

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: T29 power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

For Cougar Point Desktop: VDDIO = VCCVRM (1.8V), Vclk = 1.1V Max, Divider: 604 / 1000
For Cougar Point Mobile: VDDIO = VCCVRM (1.5V), Vclk = 1.1V Max, Divider: 332 / 1000
For Caesar-IV (BCM57765): VDDIO = XTALVDDH (3.3V), Vclk = 3.3V Max. No Divider Necessary



SYNC MASTER=K62	SYNC DATE=01/06/2013
PAGE TITLE	GREEN CLOCK
Apple Inc.	DRAWING NUMBER 051-8115 SIZE D
	REVISION 11.1.0
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Page Notes

Power aliases required by this page:
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

Signal aliases required by this page:
- =T29_CLKREQ_L
- T29_RESET_L

BOM options provided by this page:
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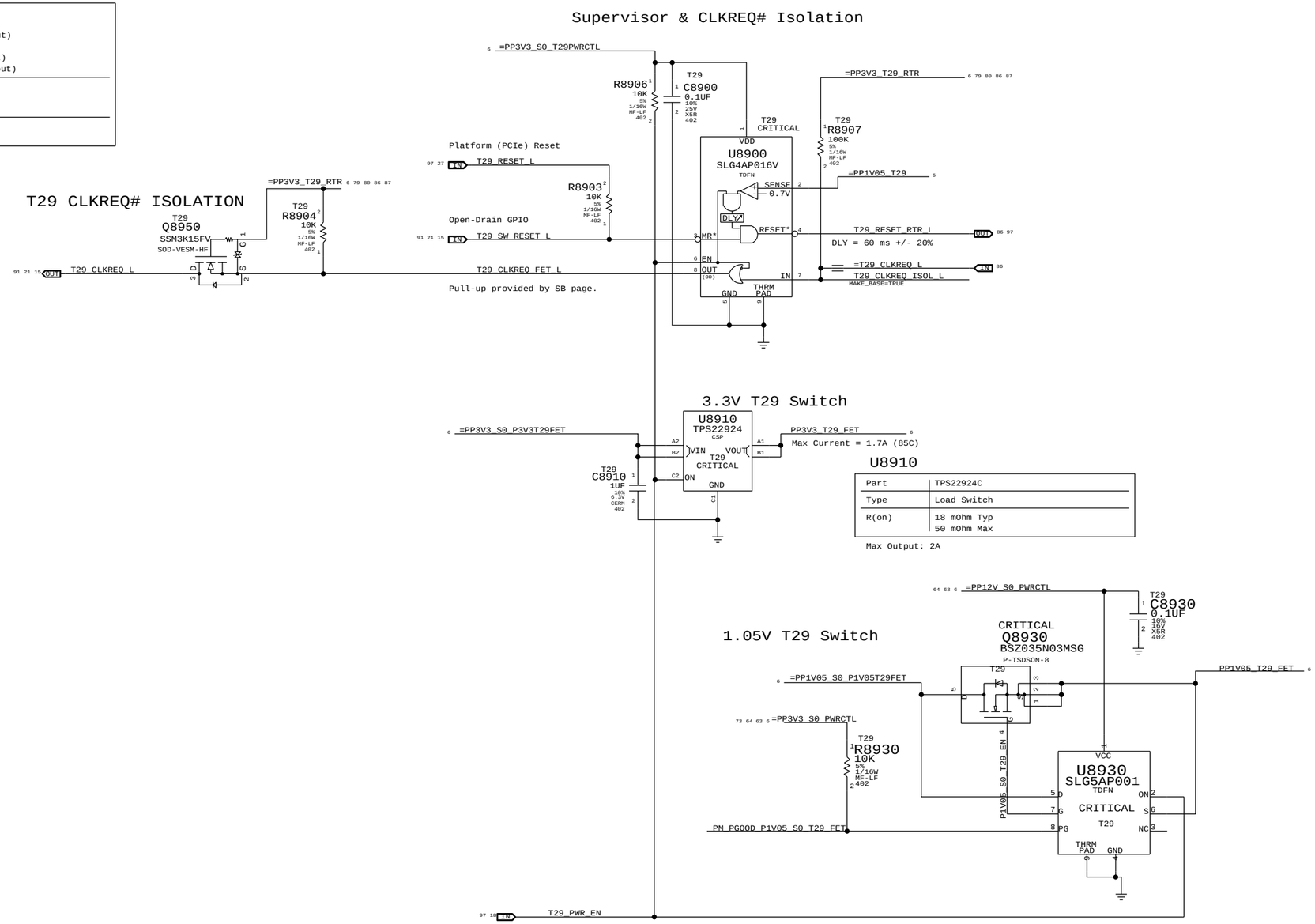

SYNC_MASTER=K62	SYNC_DATE=01/06/2011
PAGE TITLE	T29 POWER
Apple Inc.	DRAWING NUMBER 051-8115 SIZE D
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Page Notes

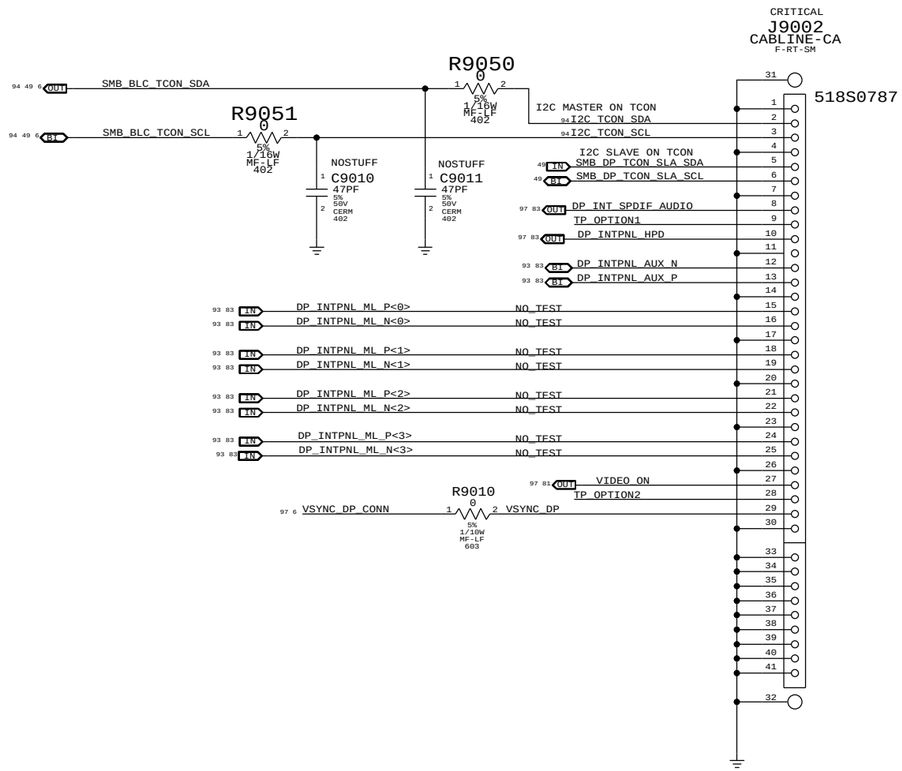
Power aliases required by this page:

- =PP12V_S0_LCD
- =PP3V3_S0_VIDEO

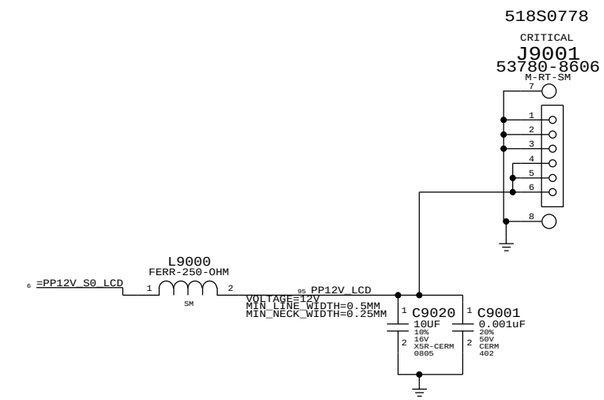
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
IG, MXM, MLB_PNL_PWR, LCD_PNL_PWR

INTERNAL DP INTERFACE

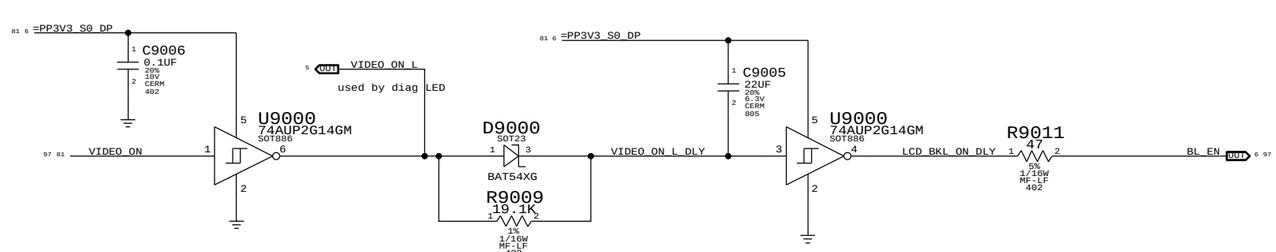


INTERNAL DP POWER



BACKLIGHT CONTROL SUPPORT

guarantee backlight is
only on when Panel has valid video



SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
Display: Int DP Connector

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

REVISION 11.1.0

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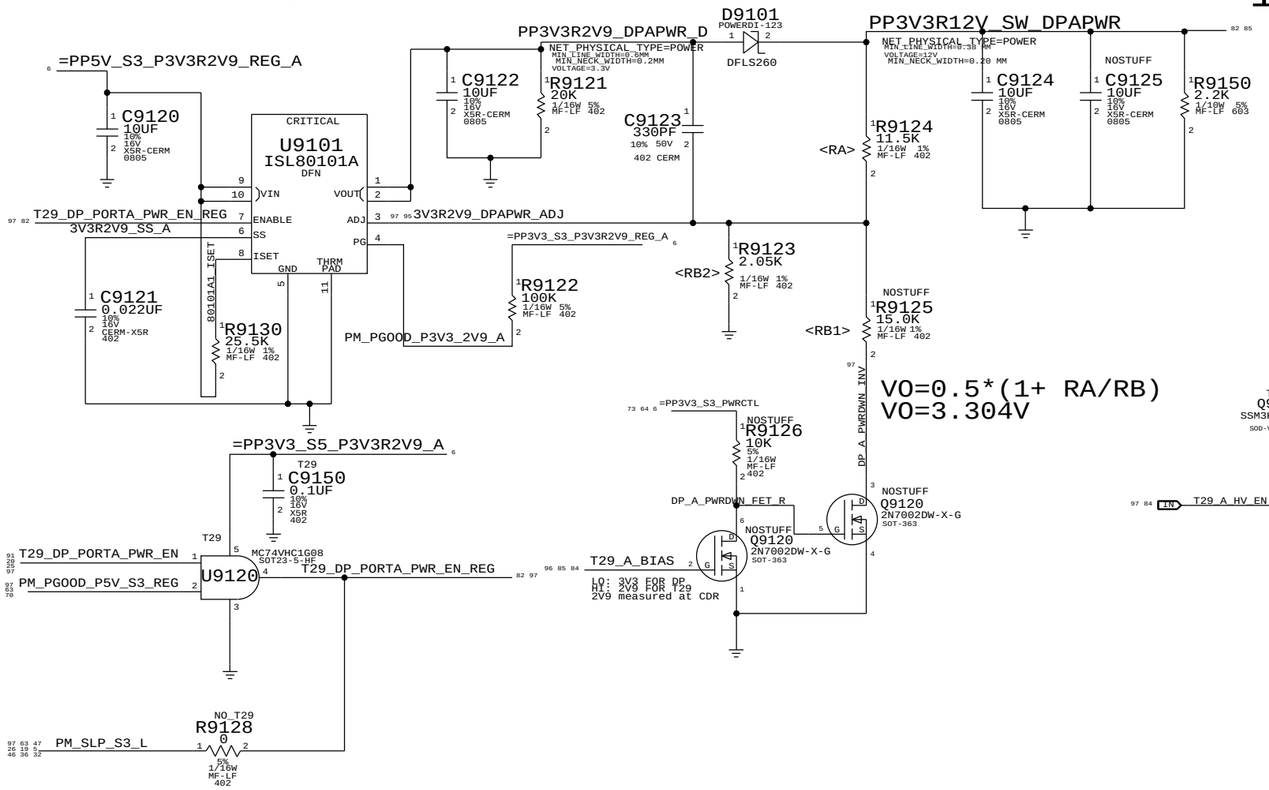
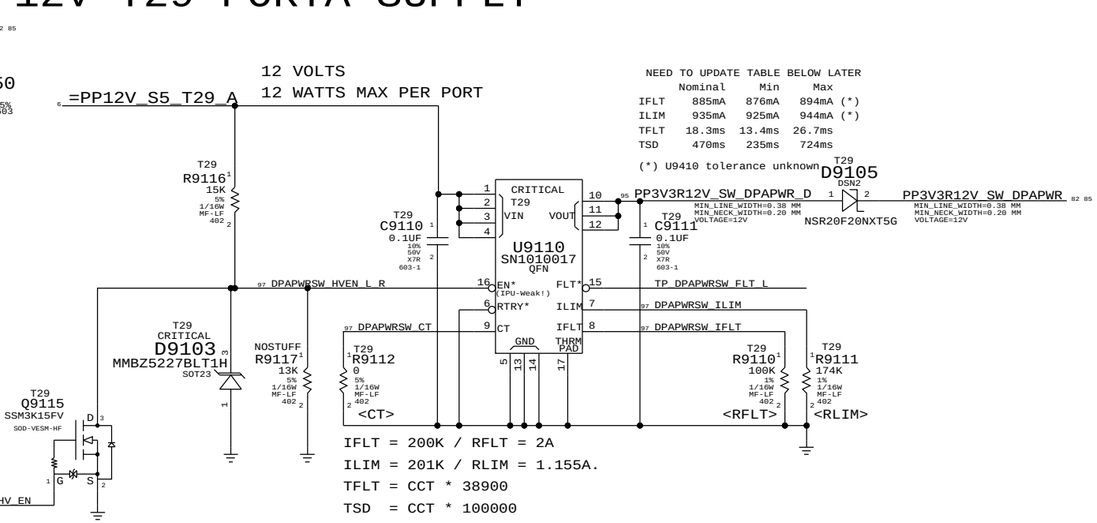
3V3(DP)/2V9(T29) PORTA SUPPLY



12V T29 PORTA SUPPLY



SYNC_MASTER=K62 SYNC_DATE=11/14/2010

PAGE TITLE
2V9/3V3/12V POWER SWITCH

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

REVISION 11.1.0

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PAGE 91 OF 110

SHEET 82 OF 98

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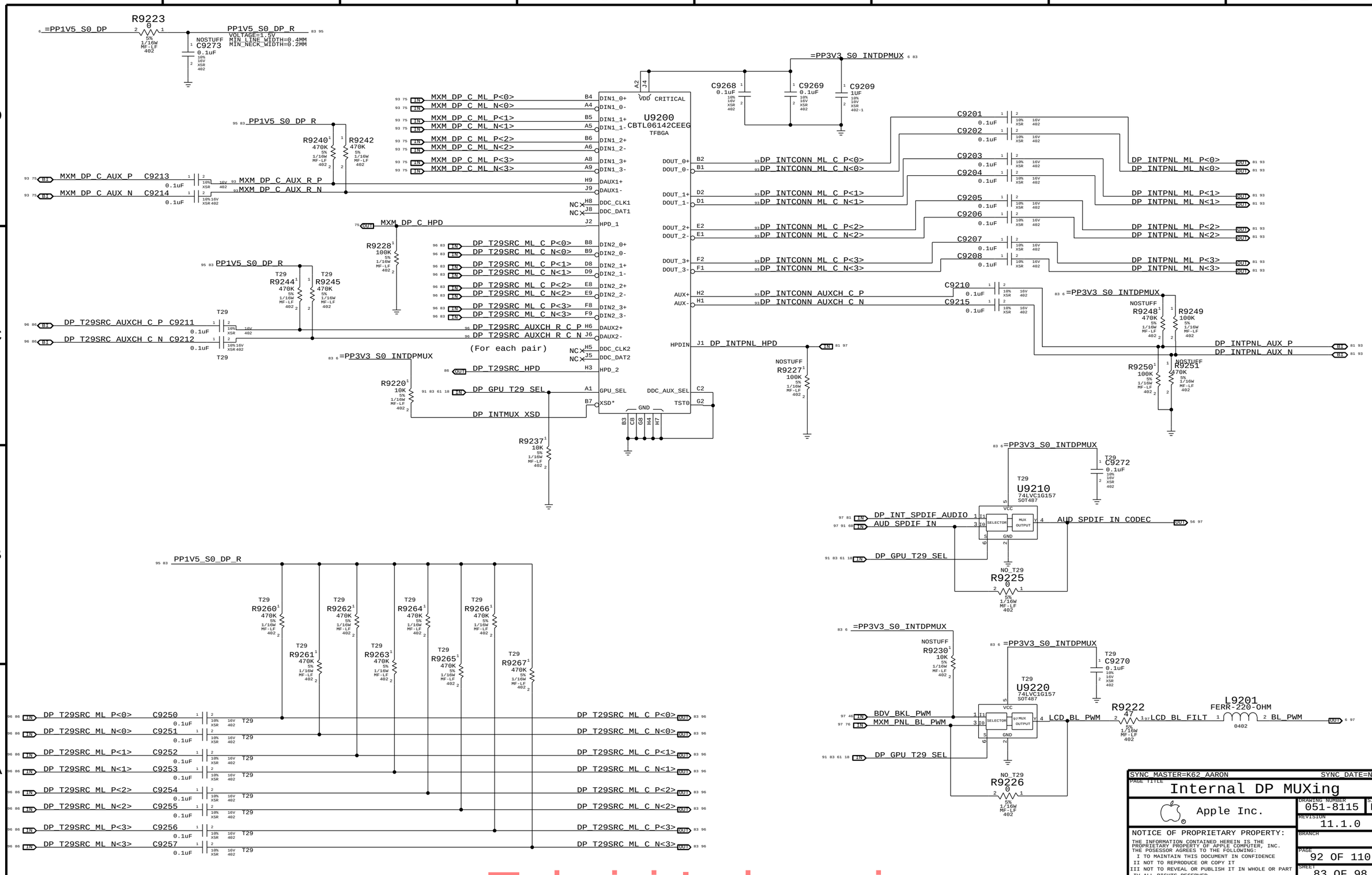

SYNC_MASTER=K62_AARON SYNC_DATE=N/A

PAGE TITLE: Internal DP MUXing

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DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

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SHEET: 83 OF 98

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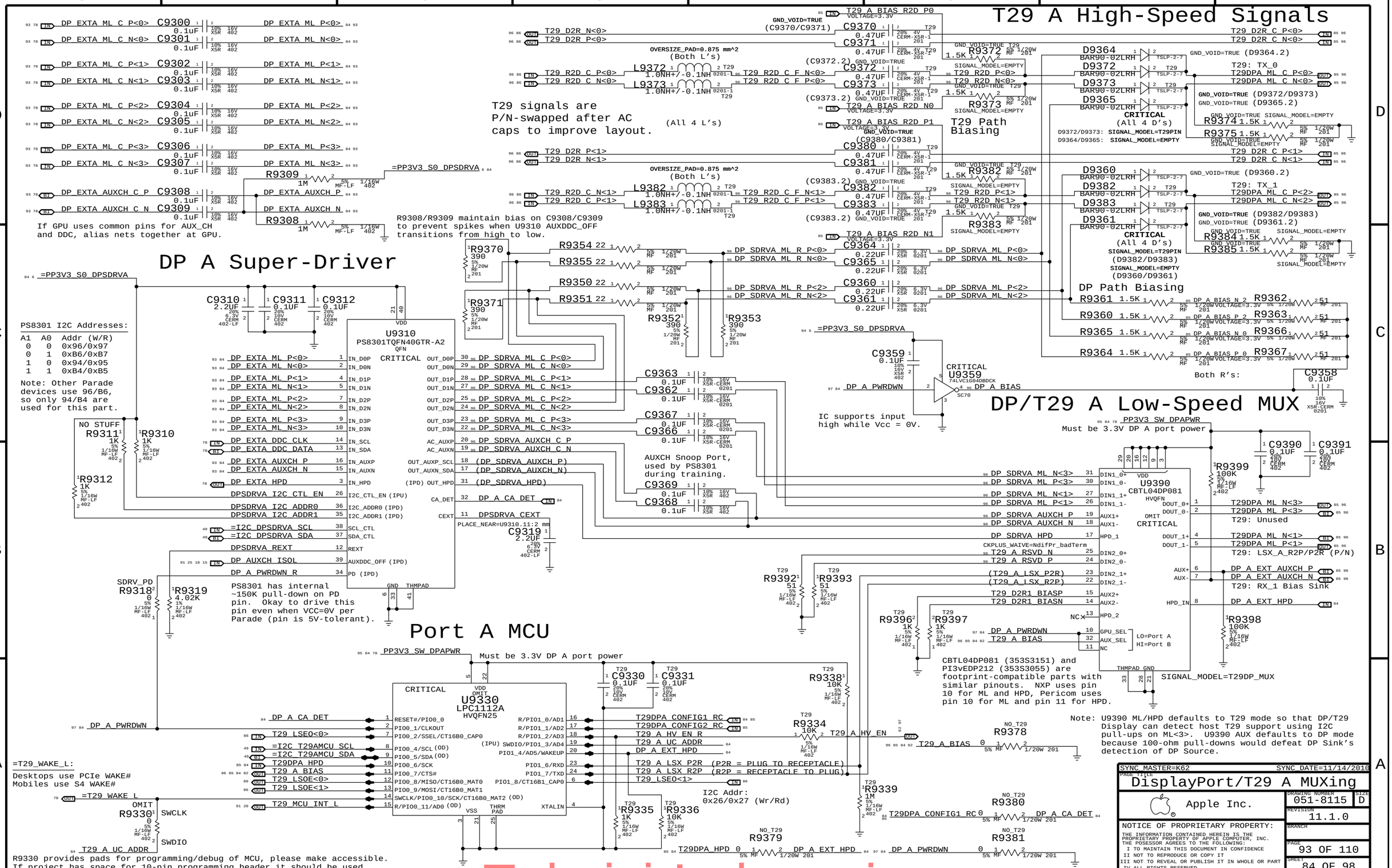

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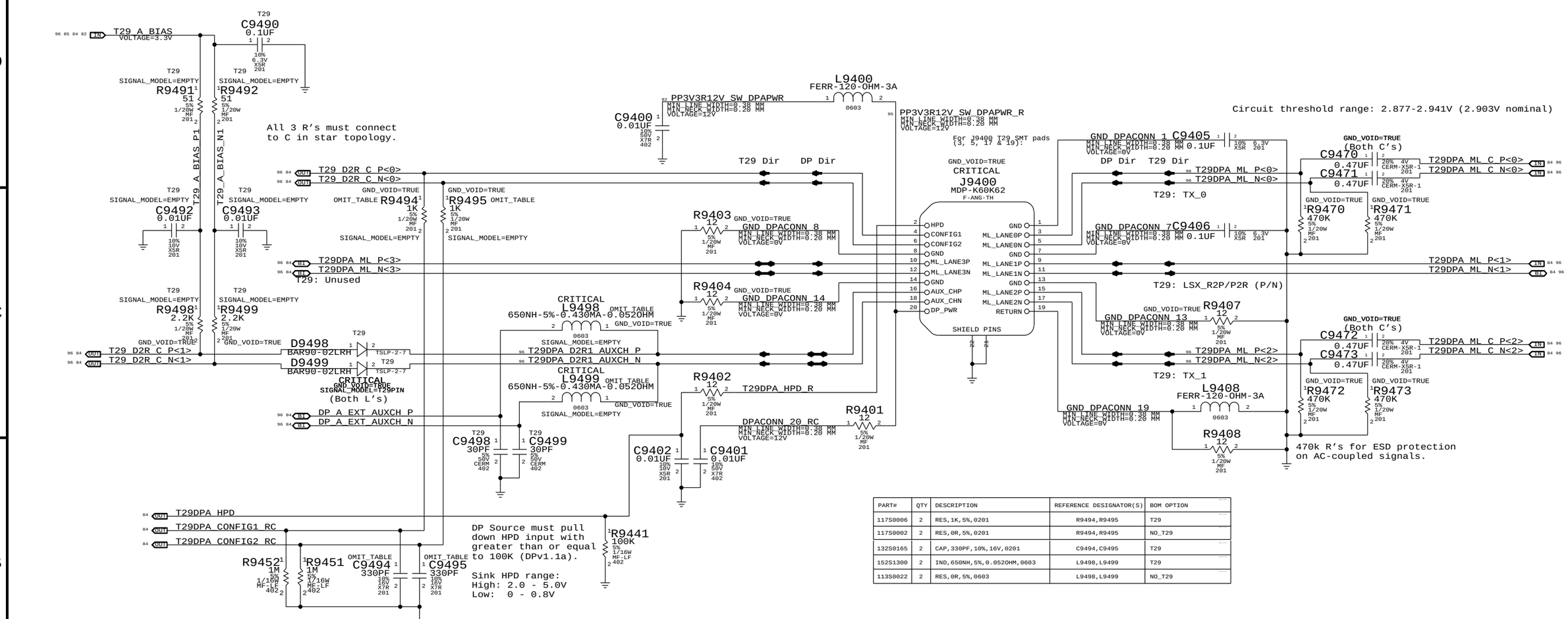
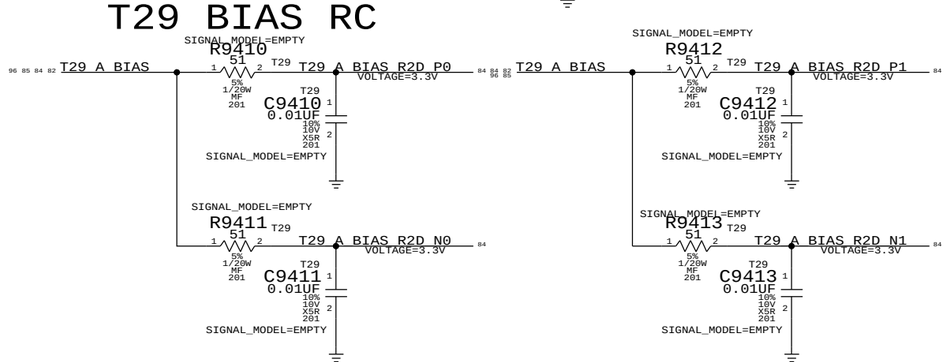
DisplayPort/T29 A Connector

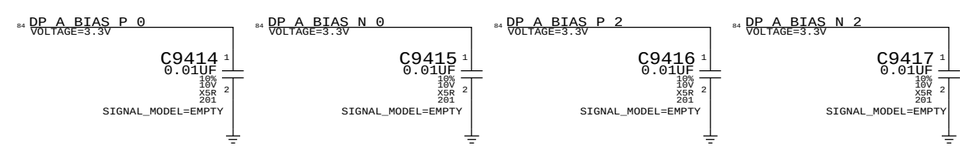


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
117S0006	2	RES,1K,5%,0201	R9494,R9495	T29
117S0002	2	RES,0R,5%,0201	R9494,R9495	NO_T29
132S0165	2	CAP,330PF,10%,16V,0201	C9494,C9495	T29
152S1300	2	IND,650NH,5%,0.052OHM,0603	L9498,L9499	T29
113S0022	2	RES,0R,5%,0603	L9498,L9499	NO_T29

T29 BIAS RC



DP BIAS CAPS



SYNC MASTER=(MASTER) SYNC DATE=(MASTER)

PAGE TITLE: DisplayPort/T29 A Connector

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

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PAGE: 94 OF 110

SHEET: 85 OF 98

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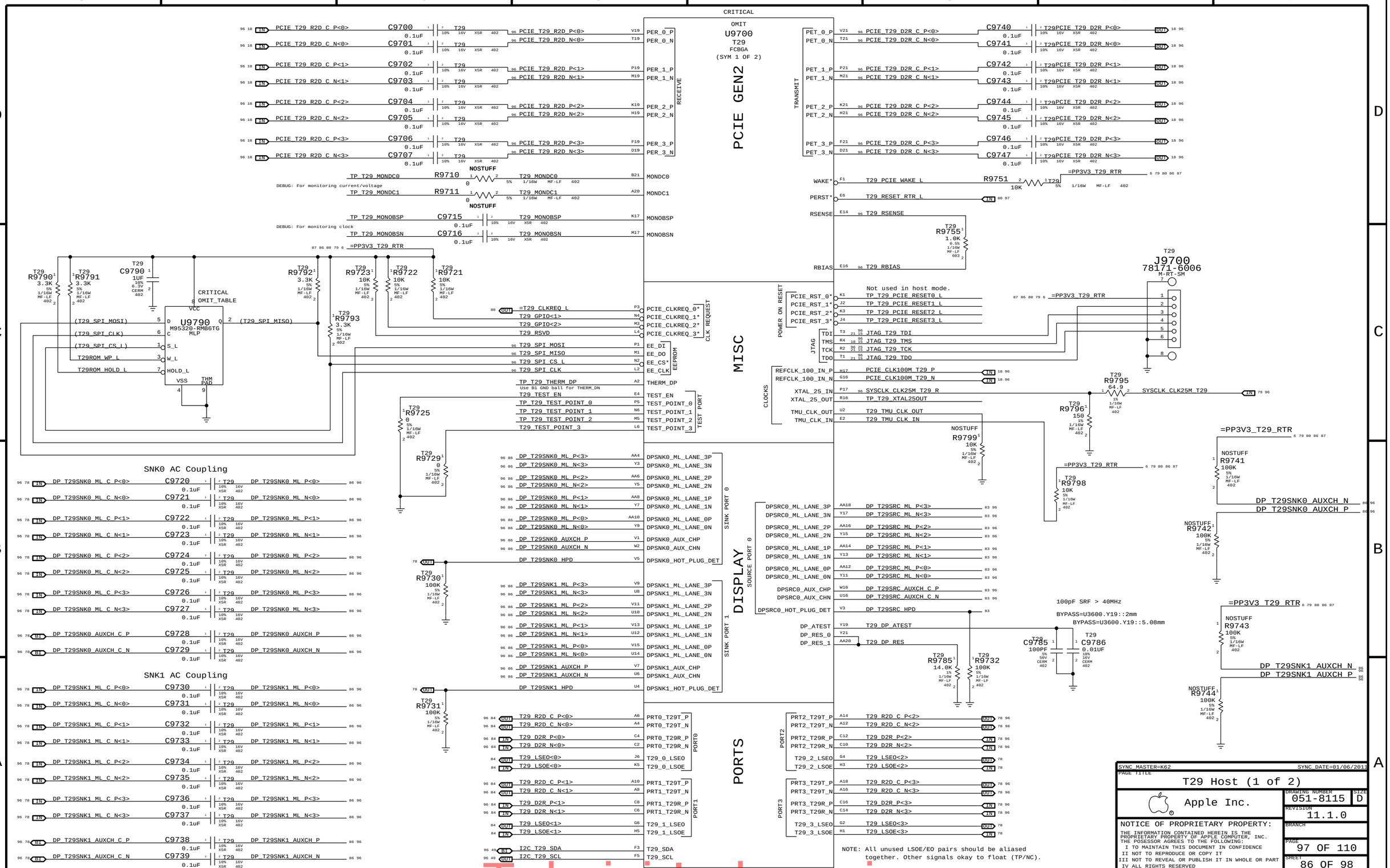

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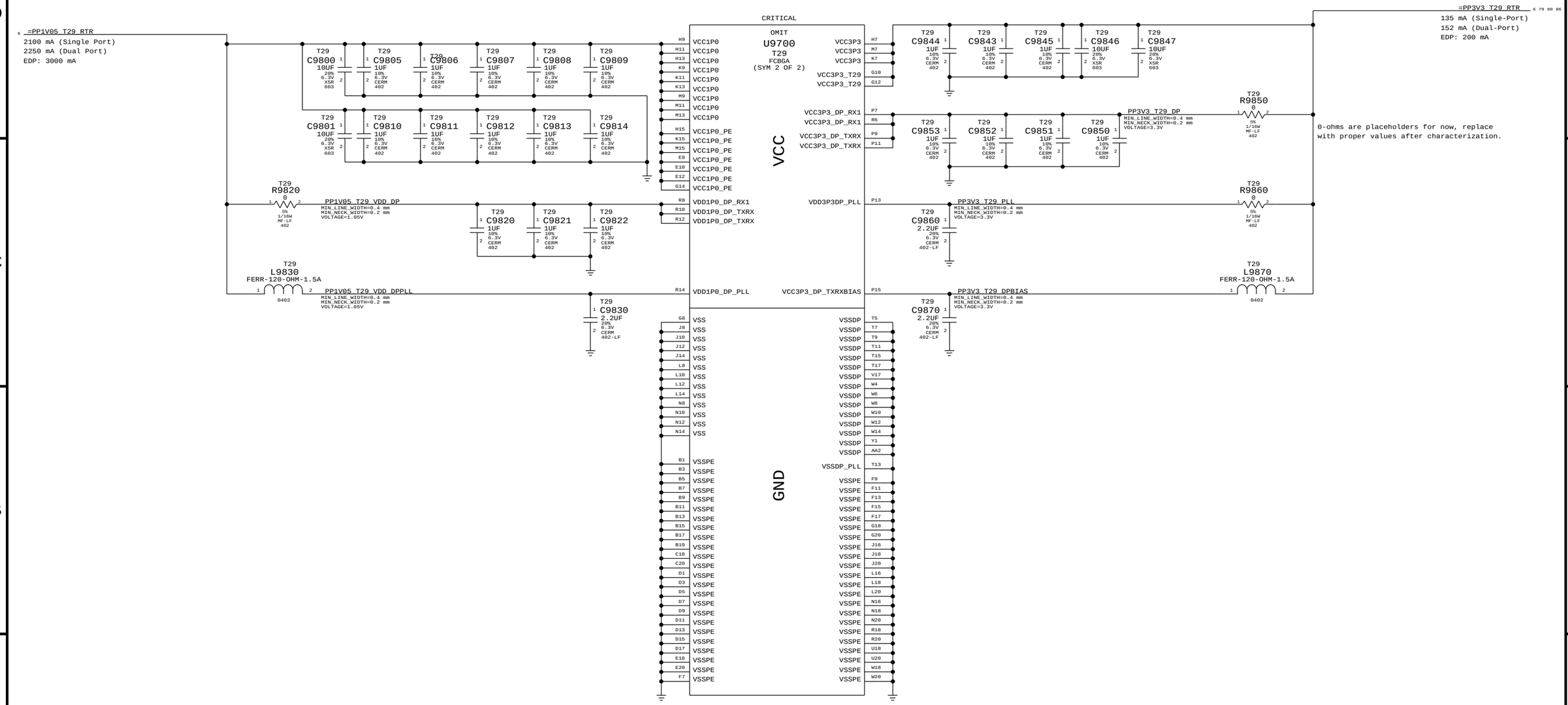

0-ohms are placeholders for now, replace with proper values after characterization.

Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: T29 Host (2 of 2)

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K60/62 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA,BGA_P1MM	MM	15.5.1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
34_OHM_SE	TOP,BOTTOM	Y	0.21 MM	0.090 MM	=STANDARD		
34_OHM_SE	*	Y	0.19 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	TOP,BOTTOM	Y	0.175 MM	0.090 MM	=STANDARD		
39_OHM_SE	*	Y	0.159 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	TOP,BOTTOM	Y	0.151 MM	0.090 MM	=STANDARD		
42_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.1 MM	0.085 MM	15 MM		
50_OHM_SE	*	Y	0.1 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD		
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
68_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
68_OHM_DIFF	ISL3,ISL6	Y	0.16 MM	0.090 MM	=STANDARD	0.13 MM	0.1 MM
68_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.090 MM	=STANDARD	0.13 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL6	Y	0.115 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL6	Y	0.099 MM	0.085 MM	12 MM	0.2 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL6	Y	0.081 MM	0.081 MM	=STANDARD	0.25 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL6	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.075 MM	=STANDARD	0.320 MM	0.15 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
POWER_WIDTH	*	Y	0.600 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
POWER_CTL	*	Y	0.300 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
3.5:1_SPACING	*	0.35 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?
6:1_SPACING	*	0.6 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.155 MM	?
2X_DIELECTRIC	TOP,BOTTOM	0.145 MM	?
3X_DIELECTRIC	*	0.230 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.215 MM	?
4X_DIELECTRIC	*	0.305 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.285 MM	?
5X_DIELECTRIC	*	0.380 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.355 MM	?
7X_DIELECTRIC	*	0.532 MM	?
7X_DIELECTRIC	TOP,BOTTOM	0.497 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	*	*	STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000
SWITCHNODE	*	0.8 MM	1000

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=DEFAULT	?
BGA_P1P5MM	*	0.15 MM	?
BGA_P2MM	*	0.2 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P1P5MM
CLK_PCIE	*	BGA	BGA_P1MM
CLK_LPC	*	BGA	BGA_P1MM
CLK_PCI	*	BGA	BGA_P1MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_CONTROL	*	*	SWITCHNODE
VR_CONTROL	VR_CONTROL	*	STANDARD
VR_CONTROL	SWITCHNODE	*	STANDARD
VR_CONTROL	GND	*	STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER	BGA_P1MM	POWER_CTL
POWER	*	POWER_WIDTH
VR_CTL_PHY	BGA_P1MM	DEFAULT
VR_CTL_PHY	*	POWER_CTL

BOARD STACK-UP

TOP	HALF OZ	SIGNAL
	0.071	PREPREG
2	TWO OZ	GND
	0.076	PREPREG
3	ONE OZ	SIGNAL
	0.370	PREPREG
4	TWO OZ	POWER
	0.101	CORE
5	TWO OZ	POWER
	0.370	PREPREG
6	ONE OZ	SIGNAL
	0.076	PREPREG
7	TWO OZ	GND
	0.071	PREPREG
BOTTOM	HALF OZ	SIGNAL

BOARD THICKNESS = 62 MIL (1.5748 mm)

SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE: K60/K62 RULE DEFINITIONS

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DRAWING NUMBER: 051-8115 SIZE: D

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=STANDARD	=STANDARD
MEM_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
MEM_34S	*	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=STANDARD	=STANDARD
MEM_68D	*	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF
MEM_42S_D	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	0.1016 MM	0.1016 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2.5:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=2:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DQ_SAMEBYTE	*	=3:1_SPACING	?
MEM_DQ_DIFFBYTE	*	=5:1_SPACING	?
MEM_DATA2MEM	*	=4:1_SPACING	?
MEM_DQS2MEM	*	=4:1_SPACING	?
MEM_2OTHER	*	=5:1_SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE0	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE1	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE2	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE3	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE4	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE5	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE6	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_BYTE7	*	MEM_DQS2MEM
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE5	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE5	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE5	MEM_DQ_BYTE5	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE5	MEM_DQ_BYTE6	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE5	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE5	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE6	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE6	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE6	MEM_DQ_BYTE6	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE6	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE6	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE7	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE7	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE7	MEM_DQ_BYTE7	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE7	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE0	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE0	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE0	MEM_DQ_BYTE0	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE1	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE2	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE3	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE4	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE5	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE6	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE0	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE1	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE1	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE1	MEM_DQ_BYTE1	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE1	MEM_DQ_BYTE2	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE1	MEM_DQ_BYTE3	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE1	MEM_DQ_BYTE4	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE1	MEM_DQ_BYTE5	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE1	MEM_DQ_BYTE6	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE1	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE1	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE2	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE2	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE2	MEM_DQ_BYTE2	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE2	MEM_DQ_BYTE3	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE2	MEM_DQ_BYTE4	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE2	MEM_DQ_BYTE5	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE2	MEM_DQ_BYTE6	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE2	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE2	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE3	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE3	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE3	MEM_DQ_BYTE3	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE3	MEM_DQ_BYTE4	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE3	MEM_DQ_BYTE5	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE3	MEM_DQ_BYTE6	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE3	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE3	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_BYTE4	MEM_CTRL	*	MEM_DATA2MEM
MEM_DQ_BYTE4	MEM_CMD	*	MEM_DATA2MEM
MEM_DQ_BYTE4	MEM_DQ_BYTE4	*	MEM_DQ_SAMEBYTE
MEM_DQ_BYTE4	MEM_DQ_BYTE5	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE4	MEM_DQ_BYTE6	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE4	MEM_DQ_BYTE7	*	MEM_DQ_DIFFBYTE
MEM_DQ_BYTE4	*	*	MEM_2OTHER

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MEM_68D	MEM_CLK	MEM_A_CLK_P<3..0>	12 32
	MEM_68D	MEM_CLK	MEM_A_CLK_N<3..0>	12 32
	MEM_39S	MEM_CTRL	MEM_A_CKE<3..0>	12 30
	MEM_39S	MEM_CTRL	MEM_A_CS_L<3..0>	12 30
	MEM_39S	MEM_CTRL	MEM_A_ODT<3..0>	12 30
	MEM_34S	MEM_CMD	MEM_A_A<15..0>	12 30
	MEM_34S	MEM_CMD	MEM_A_BA<2..0>	12 30
	MEM_34S	MEM_CMD	MEM_A_RAS_L	12 30
	MEM_34S	MEM_CMD	MEM_A_CAS_L	12 30
	MEM_34S	MEM_CMD	MEM_A_WE_L	12 30
	MEM_42S	MEM_DQ_BYTE0	MEM_A_DQ<7..0>	12 32
	MEM_42S	MEM_DQ_BYTE1	MEM_A_DQ<15..8>	12 32
	MEM_42S	MEM_DQ_BYTE2	MEM_A_DQ<23..16>	12 32
	MEM_42S	MEM_DQ_BYTE3	MEM_A_DQ<31..24>	12 32
	MEM_42S	MEM_DQ_BYTE4	MEM_A_DQ<39..32>	12 32
	MEM_42S	MEM_DQ_BYTE5	MEM_A_DQ<47..40>	12 32
	MEM_42S	MEM_DQ_BYTE6	MEM_A_DQ<55..48>	12 32
	MEM_42S	MEM_DQ_BYTE7	MEM_A_DQ<63..56>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<0>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<0>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<1>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<1>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<2>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<2>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<3>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<3>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<4>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<4>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<5>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<5>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<6>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<6>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_P<7>	12 32
	MEM_42S_D	MEM_DQS	MEM_A_DQS_N<7>	12 32
E17A	MEM_50S	PM	MEM_RESET_L	30 31 32 97

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MEM_68D	MEM_CLK	MEM_B_CLK_P<3..0>	12 32
	MEM_68D	MEM_CLK	MEM_B_CLK_N<3..0>	12 32
	MEM_39S	MEM_CTRL	MEM_B_CKE<3..0>	12 31
	MEM_39S	MEM_CTRL	MEM_B_CS_L<3..0>	12 31
	MEM_39S	MEM_CTRL	MEM_B_ODT<3..0>	12 31
	MEM_34S	MEM_CMD	MEM_B_A<15..0>	12 31
	MEM_34S	MEM_CMD	MEM_B_BA<2..0>	12 31
	MEM_34S	MEM_CMD	MEM_B_RAS_L	12 31
	MEM_34S	MEM_CMD	MEM_B_CAS_L	12 31
	MEM_34S	MEM_CMD	MEM_B_WE_L	12 31
	MEM_42S	MEM_DQ_BYTE0	MEM_B_DQ<7..0>	12 32
	MEM_42S	MEM_DQ_BYTE1	MEM_B_DQ<15..8>	12 32
	MEM_42S	MEM_DQ_BYTE2	MEM_B_DQ<23..16>	12 32
	MEM_42S	MEM_DQ_BYTE3	MEM_B_DQ<31..24>	12 32
	MEM_42S	MEM_DQ_BYTE4	MEM_B_DQ<39..32>	12 32
	MEM_42S	MEM_DQ_BYTE5	MEM_B_DQ<47..40>	12 32
	MEM_42S	MEM_DQ_BYTE6	MEM_B_DQ<55..48>	12 32
	MEM_42S	MEM_DQ_BYTE7	MEM_B_DQ<63..56>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<0>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<0>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<1>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<1>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<2>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<2>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<3>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<3>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<4>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<4>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<5>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<5>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<6>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<6>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_P<7>	12 32
	MEM_42S_D	MEM_DQS	MEM_B_DQS_N<7>	12 32

MEMORY MISC PROPERTIES

VOLTAGE	NET_TYPE PHYSICAL	NET_TYPE SPACING	VOLTAGE		
	MEM_POWER_PHY	MEM_POWER		CPU_DIMM_VREF_A	
	MEM_POWER_PHY	MEM_POWER		CPU_DIMM_VREF_B	
E16A	MEM_POWER_PHY	MEM_POWER		CPU_DDR_VREF	11 28
E16B	MEM_POWER_PHY	MEM_POWER		VREFMARGIN_DIMMA_DACOUT	28
E16C	MEM_POWER_PHY	MEM_POWER		VREFMARGIN_DIMMA_OPFB	28
E17A	MEM_POWER_PHY	MEM_POWER		VREFMARGIN_DIMMA_DQ	28
E17B	MEM_POWER_PHY	MEM_POWER		CPU_DIMM_VREF_A_SW	
E17C	MEM_POWER_PHY	MEM_POWER		VREFMARGIN_DIMMB_DACOUT	28
E17D	MEM_POWER_PHY	MEM_POWER		VREFMARGIN_DIMMB_OPFB	28
E17E	MEM_POWER_PHY	MEM_POWER		VREFMARGIN_DIMMB_DQ	28
E17F	MEM_POWER_PHY	MEM_POWER		CPU_DIMM_VREF_B_SW	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_POWER_WIDTH	*	Y	0.500 MM	0.250 MM	=STANDARD	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_POWER_PHY	*	MEM_POWER_WIDTH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_POWER	*	=3:1_SPACING	?

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PAGE TITLE
Memory Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=4X_DIELECTRIC	?
CLK_PCIE	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4:1_SPACING	?

CPU

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_RCOMP_PHY	*	Y	0.254 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP	*	0.2 MM	?
CPU_RCOMP	*	0.2 MM	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=6:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=6:1_SPACING	?

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SATA				
1B9D	SATA_90D	SATA	SATA_SSD_R2D_C_P	18 42
1B9E	SATA_90D	SATA	SATA_SSD_R2D_C_N	18 42
1B9F	SATA_90D	SATA	SATA_SSD_R2D_P	42
1BA0	SATA_90D	SATA	SATA_SSD_R2D_N	42
1BA1	SATA_90D	SATA	SATA_SSD_D2R_P	18 42
1BA2	SATA_90D	SATA	SATA_SSD_D2R_N	18 42
1BA3	SATA_90D	SATA	SATA_SSD_D2R_C_P	42
1BA4	SATA_90D	SATA	SATA_SSD_D2R_C_N	42
PCIE				
1B1C	PCIE_85D	PCIE	PCIE_USB3_1_R2D_P	
1B1D	PCIE_85D	PCIE	PCIE_USB3_1_R2D_N	
1B1E	PCIE_85D	PCIE	PCIE_USB3_1_R2D_C_P	
1B1F	PCIE_85D	PCIE	PCIE_USB3_1_R2D_C_N	
1B20	PCIE_85D	PCIE	PCIE_USB3_1_D2R_P	
1B21	PCIE_85D	PCIE	PCIE_USB3_1_D2R_N	
1B22	PCIE_85D	PCIE	PCIE_USB3_1_D2R_C_P	
1B23	PCIE_85D	PCIE	PCIE_USB3_1_D2R_C_N	
1B2C	PCIE_85D	PCIE	PCIE_USB3_2_R2D_P	
1B2D	PCIE_85D	PCIE	PCIE_USB3_2_R2D_N	
1B2E	PCIE_85D	PCIE	PCIE_USB3_2_R2D_C_P	
1B2F	PCIE_85D	PCIE	PCIE_USB3_2_R2D_C_N	
1B30	PCIE_85D	PCIE	PCIE_USB3_2_D2R_P	
1B31	PCIE_85D	PCIE	PCIE_USB3_2_D2R_N	
1B32	PCIE_85D	PCIE	PCIE_USB3_2_D2R_C_P	
1B33	PCIE_85D	PCIE	PCIE_USB3_2_D2R_C_N	
CPU ITP				
1B3A	CPU_50S	CPU_ITP	XDP_BPM_L<7..0>	11 25
1B3B	CPU_50S	CPU_ITP	CPU_CFG<17..0>	10 15 25
1B3C	CPU_50S	CPU_ITP	XDP_OBSDATA_B<3..0>	25
1B3D	CPU_50S	CPU_ITP	XDP_CPU_CFG<0>	25
1B3E	CPU_50S	CPU_ITP	XDP_CPU_TDO	11 25
1B3F	CPU_50S	CPU_ITP	XDP_CPU_TDI	11 25
1B40	CPU_50S	CPU_ITP	XDP_CPU_TMS	11 25
1B41	CPU_50S	CPU_ITP	XDP_CPU_TCK	11 25
1B50	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	11 25
CPU_MISC				
	CPU_RCOMP_PHY	CPU_RCOMP	CPU_PEG_COMP	10

ANY OTHER LYNNFIELD CONSTRAINTS NOT COVERED ON PAGES 101 AND 107 SHOULD GO ON THIS PAGE TOO

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE GRAPHICS				
	PCIE_85D	PCIE	PEG_R2D_C_P<15..0>	9 77
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0>	9 77
	PCIE_85D	PCIE	PEG_D2R_P<15..0>	9 77
	PCIE_85D	PCIE	PEG_D2R_N<15..0>	9 77
	PCIE_85D	PCIE	MXM_PCIE_R2D_P<7..0>	75 77
	PCIE_85D	PCIE	MXM_PCIE_R2D_N<7..0>	75 77
	PCIE_85D	PCIE	MXM_PCIE_D2R_P<7..0>	75 77
	PCIE_85D	PCIE	MXM_PCIE_D2R_N<7..0>	75 77
PCIE I/O				
	PCIE_85D	PCIE	PCIE_MINI_R2D_P	33
	PCIE_85D	PCIE	PCIE_MINI_R2D_N	33
	PCIE_85D	PCIE	PCIE_MINI_R2D_C_P	18 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_C_N	18 33
	PCIE_85D	PCIE	PCIE_MINI_D2R_P	18 33
	PCIE_85D	PCIE	PCIE_MINI_D2R_N	18 33
	PCIE_85D	PCIE	PCIE_FW_R2D_P	39
	PCIE_85D	PCIE	PCIE_FW_R2D_N	39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	18 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_P	18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_N	18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	39
DMI				
1B1A	CLK_PCIE_90D	CLK_PCIE	DMI_MIDBUS_CLK100M_N	
1B1B	CLK_PCIE_90D	CLK_PCIE	DMI_MIDBUS_CLK100M_P	
1B1C	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	11 18
1B1D	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	11 18
	PCIE_85D	PCIE	DMI_S2N_P<3..0>	10 19
	PCIE_85D	PCIE	DMI_S2N_N<3..0>	10 19
	PCIE_85D	PCIE	DMI_N2S_P<3..0>	10 19
	PCIE_85D	PCIE	DMI_N2S_N<3..0>	10 19
PCIE REF CLOCKS				
	CLK_PCIE_90D	CLK_PCIE	GPU_CLK100M_PCIE_P	9
	CLK_PCIE_90D	CLK_PCIE	GPU_CLK100M_PCIE_N	9
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_MINI_P	18 33
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_MINI_N	18 33
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	18 39
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	18 39
	ENET_100D	ENET_MII	PCIE_CLK100M_ENET_P	18 37
	ENET_100D	ENET_MII	PCIE_CLK100M_ENET_N	18 37
SATA				
	SATA_90D	SATA	SATA_HDD_R2D_C_P	18 42
	SATA_90D	SATA	SATA_HDD_R2D_C_N	18 42
	SATA_90D	SATA	SATA_HDD_R2D_P	42
	SATA_90D	SATA	SATA_HDD_R2D_N	42
	SATA_90D	SATA	SATA_HDD_D2R_P	18 42
	SATA_90D	SATA	SATA_HDD_D2R_N	18 42
	SATA_90D	SATA	SATA_HDD_D2R_C_P	42
	SATA_90D	SATA	SATA_HDD_D2R_C_N	42
	SATA_90D	SATA	SATA_ODD_R2D_C_P	18 42
	SATA_90D	SATA	SATA_ODD_R2D_C_N	18 42
	SATA_90D	SATA	SATA_ODD_R2D_P	42
	SATA_90D	SATA	SATA_ODD_R2D_N	42
	SATA_90D	SATA	SATA_ODD_D2R_P	18 42
	SATA_90D	SATA	SATA_ODD_D2R_N	18 42
	SATA_90D	SATA	SATA_ODD_D2R_C_P	42
	SATA_90D	SATA	SATA_ODD_D2R_C_N	42
CLOCKS				
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_DMI_P	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_DMI_N	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	18 26
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	18 26
	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	18 25
	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	18 25
	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	11 18
	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	11 18
1B37	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	25
1B38	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	25
UNUSED CLOCKS				
1B39	CLK_PCIE_90D	CLK_PCIE	TP_CLK133M_PCH_N	26
1B3A	CLK_PCIE_90D	CLK_PCIE	TP_CLK133M_PCH_P	26
UNUSED PCIE				
1B3B	PCIE_85D	PCIE	MXM_PCIE_R2D_P<8..15>	75 77
1B3C	PCIE_85D	PCIE	MXM_PCIE_R2D_N<8..15>	75 77
1B3D	PCIE_85D	PCIE	MXM_PCIE_D2R_P<8..15>	75 77
1B3E	PCIE_85D	PCIE	MXM_PCIE_D2R_N<8..15>	75 77

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

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PCIE/DMI/FDI/SATA CONSTRAINTS

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PCH CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH	*	=4:1_SPACING	?
COMP_PCH	*	0.2 MM	?
ITP_PCH	*	0.2 MM	?

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

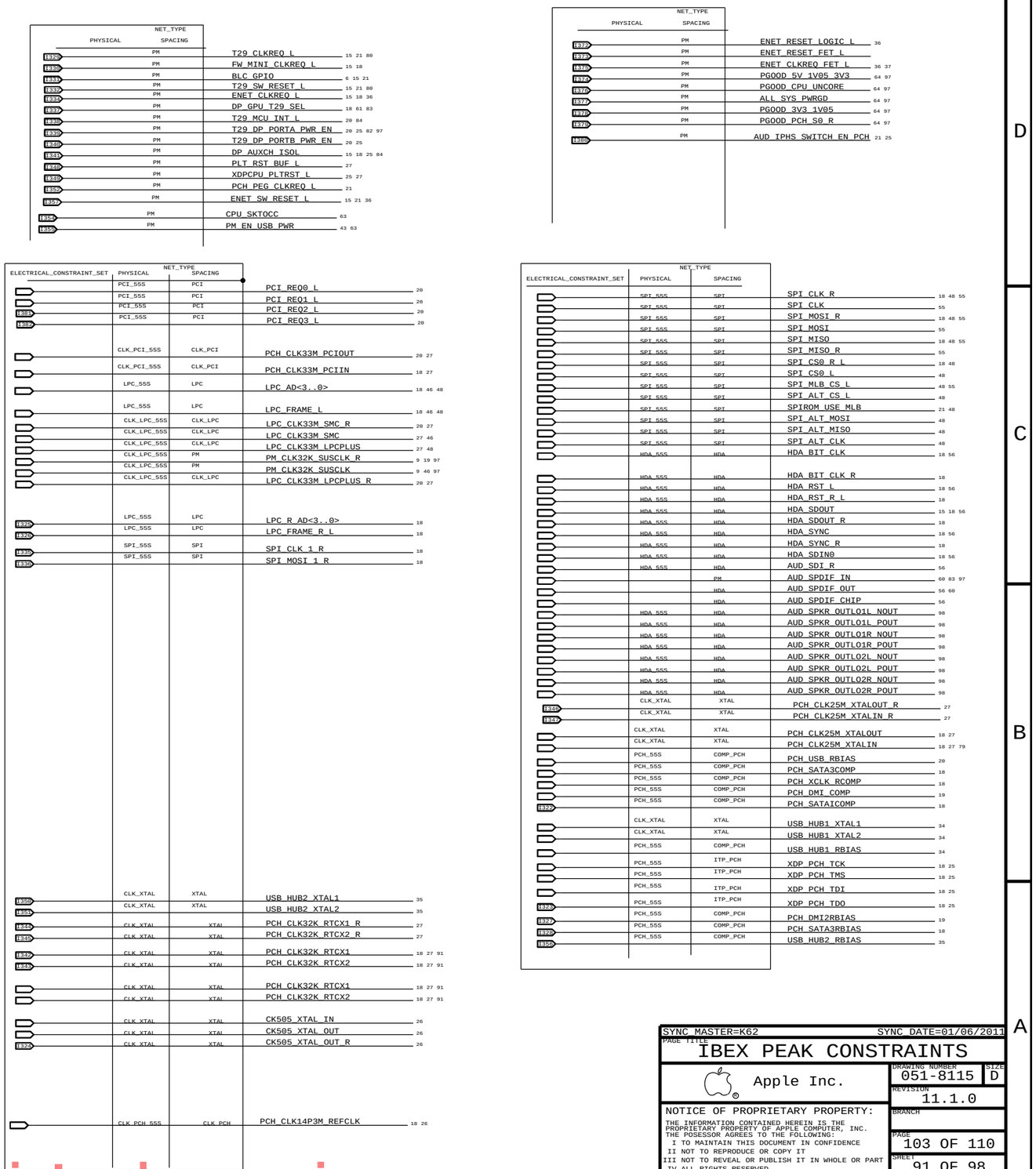
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

XTAL Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?



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CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MII	*	0.3 MM	?
ENET_SE	*	=STANDARD	?

SOURCE:BROADCOM 5764M-DS04-RDS. PAGE 38

CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF	*	0.6 MM	?
ENET_DIFF2DIFF	*	=3:1_SPACING	?
ENET_2OTHER	*	=50MIL_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
50MIL_SPACING	*	1.27 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF
ENET_DIFF_T	*	*	ENET_2OTHER

CAESAR IV (SD) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD	*	=3:1_SPACING	?

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

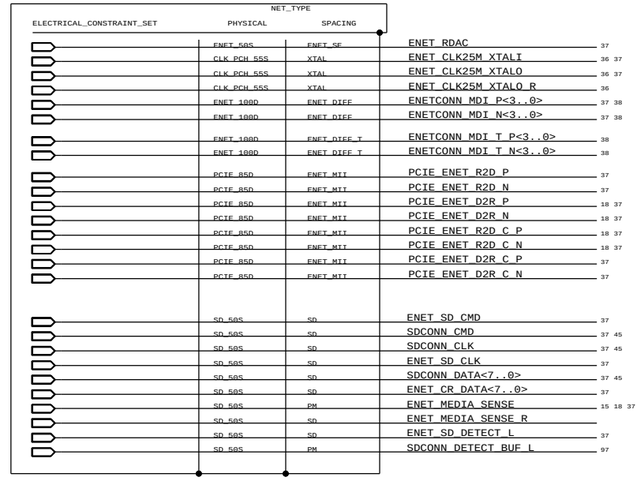
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

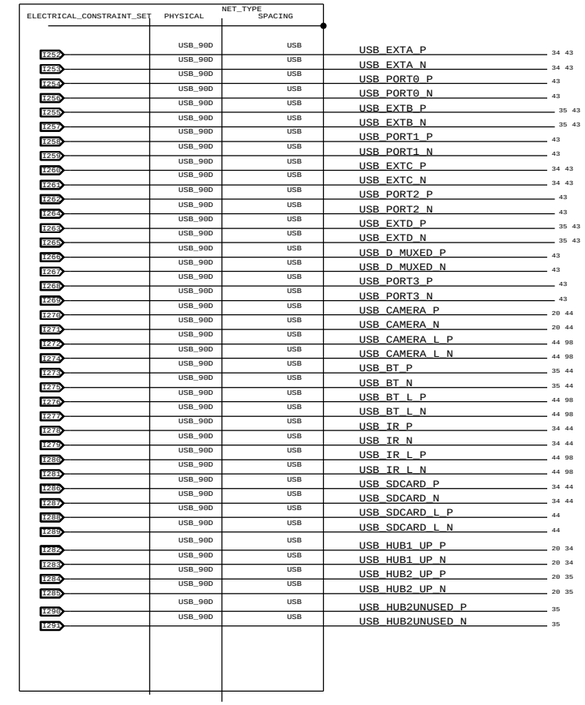
USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

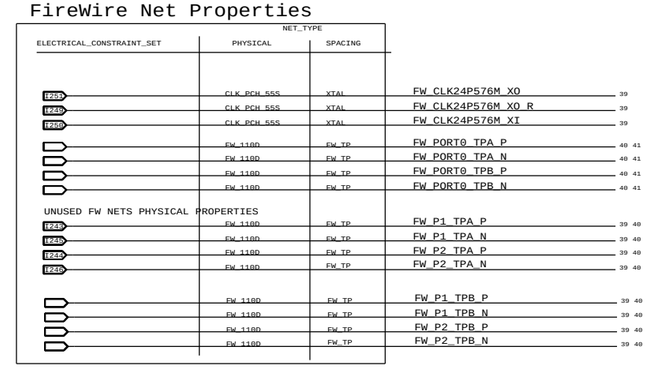
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?





FireWire Net Properties



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GRAPHICS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3:1_SPACING	?

USE 5X_DIELECTRIC IN K62

PAIRS SHOULD BE WITHIN 100 MILS OF CLOCK LENGTH.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

ELECTRICAL_CONSTRAINT_SET
ASSINGED IN CONT. MGR.

	PHYSICAL	SPACING	NET_TYPE	
	DP_85D	DISPLAYPORT	DP_INTCONN_ML_C_P<3..0>	83
I160	DP_85D	DISPLAYPORT	DP_INTCONN_ML_C_N<3..0>	83
I174	DP_85D	DISPLAYPORT	DP_INTCONN_AUXCH_C_P	83
	DP_85D	DISPLAYPORT	DP_INTCONN_AUXCH_C_N	83
	DP_85D	DISPLAYPORT	DP_INTPNL_ML_P<3..0>	81 83
I153	DP_85D	DISPLAYPORT	DP_INTPNL_ML_N<3..0>	81 83
I154	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_P	81 83
	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_N	81 83
	DP_85D	DISPLAYPORT	DP_EXTA_ML_P<3..0>	84
I181	DP_85D	DISPLAYPORT	DP_EXTA_ML_N<3..0>	84
I180	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_P	84
I188	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_N	84
I18	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_P<3..0>	78 84
I174	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_N<3..0>	78 84
I173	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	78 84
I172	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	78 84
I175	DP_85D	DISPLAYPORT	DP_EXTB_ML_P<3..0>	
I193	DP_85D	DISPLAYPORT	DP_EXTB_ML_N<3..0>	
I192	DP_85D	DISPLAYPORT	DP_EXTB_AUXCH_P	
I190	DP_85D	DISPLAYPORT	DP_EXTB_AUXCH_N	
I194	DP_85D	DISPLAYPORT	DP_EXTB_ML_C_P<3..0>	
I195	DP_85D	DISPLAYPORT	DP_EXTB_ML_C_N<3..0>	
I196	DP_85D	DISPLAYPORT	DP_EXTB_AUXCH_C_P	
I189	DP_85D	DISPLAYPORT	DP_EXTB_AUXCH_C_N	
I197	DP_85D	DISPLAYPORT	MXM_DP_B_ML_P<3..0>	75 78
I199	DP_85D	DISPLAYPORT	MXM_DP_B_ML_N<3..0>	75 78
I200	DP_85D	DISPLAYPORT	MXM_DP_B_AUX_P	75 78
I203	DP_85D	DISPLAYPORT	MXM_DP_B_AUX_N	75 78
I202	DP_85D	DISPLAYPORT	MXM_DP_C_ML_P<3..0>	75 83
I201	DP_85D	DISPLAYPORT	MXM_DP_C_ML_N<3..0>	75 83
I204	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_P	75 83
I205	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_N	75 83
I206	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_R_P	83
I241	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_R_N	83
I242	DP_85D	DISPLAYPORT	MXM_DP_D_ML_P<3..0>	75 78
P207	DP_85D	DISPLAYPORT	MXM_DP_D_ML_N<3..0>	75 78
P208	DP_85D	DISPLAYPORT	MXM_DP_D_AUX_P	75 78
P209	DP_85D	DISPLAYPORT	MXM_DP_D_AUX_N	75 78
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UNUSED VIDEO NET PHYSICAL CONSTRAINTS

	DP_85D	DISPLAYPORT	MXM_LVDS_A_CLK_P	76 78
	DP_85D	DISPLAYPORT	MXM_LVDS_A_CLK_N	76 78
	DP_85D	DISPLAYPORT	MXM_LVDS_B_CLK_P	76 78
	DP_85D	DISPLAYPORT	MXM_LVDS_B_CLK_N	76 78
	DP_85D	DISPLAYPORT	MXM_LVDS_A_DATA_P<3..0>	76 78
	DP_85D	DISPLAYPORT	MXM_LVDS_A_DATA_N<3..0>	76 78
	DP_85D	DISPLAYPORT	MXM_LVDS_B_DATA_P<3..0>	76 78
	DP_85D	DISPLAYPORT	MXM_LVDS_B_DATA_N<3..0>	76 78

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SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
THERMAL	POWER	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR
SNS_DIFF	*	1:1_DIFFPAIR

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	49
	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	49
	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	49
	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	49
	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	49
	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	49
	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	49
	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	49
	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	49 94
	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	49 94
	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	49 94
	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	49 94
	SMB_55S	SMB	SMBUS_PCH_CLK	18 49
	SMB_55S	SMB	SMBUS_PCH_DATA	18 49
	SMB_55S	SMB	SML_PCH_0_CLK	18 49
	SMB_55S	SMB	SML_PCH_0_DATA	18 49
	SMB_55S	SMB	SML_PCH_1_CLK	18 49
	SMB_55S	SMB	SML_PCH_1_DATA	18 49
	CLK_XTAL	XTAL	SMC_EXTAL	46 47
	CLK_XTAL	XTAL	SMC_XTAL	46 47
I254	SMB_55S	SMB	I2C_VREFMRGN_DIMMA_SCL	28
I253	SMB_55S	SMB	I2C_VREFMRGN_DIMMA_SDA	28
I255	SMB_55S	SMB	I2C_VREFMRGN_DIMMB_SCL	28
I256	SMB_55S	SMB	I2C_VREFMRGN_DIMMB_SDA	28
I265	SMB_55S	SMB	SMB_BLC_TCON_SCL	6 49 81
I264	SMB_55S	SMB	SMB_BLC_TCON_SDA	6 49 81
I268	SMB_55S	SMB	I2C_TCON_SCL	81
I269	SMB_55S	SMB	I2C_TCON_SDA	81
I266	SMB_55S	SMB	SMB_BLC_PCH_SCL_R	6
I267	SMB_55S	SMB	SMB_BLC_PCH_SDA_R	6

SMC THERMAL NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	THERM_DIFF	THERMAL	SNS_T1_1_P	52
	THERM_DIFF	THERMAL	SNS_T1_1_N	52
	THERM_DIFF	THERMAL	SNS_T2_DP2	52
	THERM_DIFF	THERMAL	SNS_T2_DN2	52
I208	THERM_DIFF	THERMAL	SNS_T1_2_P	52
I208	THERM_DIFF	THERMAL	SNS_T1_2_N	52
I207	THERM_DIFF	THERMAL	SNS_T1_3_P	52
I208	THERM_DIFF	THERMAL	SNS_T1_3_N	52
I210	THERM_DIFF	THERMAL	SNS_T1_4_P	52
I210	THERM_DIFF	THERMAL	SNS_T1_4_N	52
I210	THERM_DIFF	THERMAL	SNS_T1_5_P	52
I210	THERM_DIFF	THERMAL	SNS_T1_5_N	52
I210	THERM_DIFF	THERMAL	SNS_T1_6_P	52
I210	THERM_DIFF	THERMAL	SNS_T1_6_N	52
I210	THERM_DIFF	THERMAL	SNS_T1_7_P	52
I210	THERM_DIFF	THERMAL	SNS_T1_7_N	52
I220	THERM_DIFF	THERMAL	SNS_CPU_THERMD_P	10 52
I220	THERM_DIFF	THERMAL	SNS_CPU_THERMD_N	10 52
I219	THERM_DIFF	THERMAL	SNS_LCD_H_P	52
I219	THERM_DIFF	THERMAL	SNS_LCD_H_N	52
	THERM_DIFF	THERMAL	SNS_ODD_P	52 98
	THERM_DIFF	THERMAL	SNS_ODD_N	52 98
	THERM_DIFF	THERMAL	SNS_CPU_H_P	52
	THERM_DIFF	THERMAL	SNS_CPU_H_N	52
I222	THERM_DIFF	THERMAL	SNS_SKIN_RIGHT_P	52 98
I222	THERM_DIFF	THERMAL	SNS_SKIN_RIGHT_N	52 98
	THERM_DIFF	THERMAL	SNS_SKIN_LEFT_P	44 52 98
	THERM_DIFF	THERMAL	SNS_SKIN_LEFT_N	44 52 98
	THERM_DIFF	THERMAL	SNS_AMB_P	52 54 98
	THERM_DIFF	THERMAL	SNS_AMB_N	52 54 98
	THERM_DIFF	THERMAL	SNS_MXM_P	52
	THERM_DIFF	THERMAL	SNS_MXM_N	52
		THERMAL	HDD_OOB_TEMP_FILT	42 51 98
		THERMAL	HDD_OOB_TEMP_FB	42
		THERMAL	HDD_OOB_TEMP_R	51
		THERMAL	SMC_HDD_OOB_TEMP	46 51

SMC VOLTAGE/CURRENT NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	THERM_DIFF	THERMAL	SNS_I_MXM_P	50
	THERM_DIFF	THERMAL	SNS_I_MXM_N	50
	THERM_DIFF	THERMAL	SNS_DIMM_1V5_P	50
	THERM_DIFF	THERMAL	SNS_DIMM_1V5_N	50
	SNS_DIFF	THERMAL	VR_ISNS_VCORE_P	50 95
	SNS_DIFF	THERMAL	VR_ISNS_VCORE_N	50 95
	SNS_DIFF	THERMAL	VR_ISNS_VAXG_P	50 95
	SNS_DIFF	THERMAL	VR_ISNS_VAXG_N	50 95
I243	SNS_DIFF	THERMAL	VR_ISNS_1V05_P	95
I244	SNS_DIFF	THERMAL	VR_ISNS_1V05_N	95
I245	THERM_DIFF	THERMAL	SNS_CPU_1V5_P	50
I246	THERM_DIFF	THERMAL	SNS_CPU_1V5_N	50
I247	THERM_DIFF	THERMAL	SNS_VCCSA_P	50
I248	THERM_DIFF	THERMAL	SNS_VCCSA_N	50
I263	THERM_DIFF	THERMAL	SNS_1V05_PCH_P	50
I262	THERM_DIFF	THERMAL	SNS_1V05_PCH_N	50
I230		THERMAL	GND_SMC_AVSS	46 47 50 94
I234		THERMAL	SMC_CPU_1V5_ISENSE	46 50
I236		THERMAL	SMC_CPU_1V5_ISENSE_R	50
I232		THERMAL	SMC_CPU_1V5_VSENSE	46 50
I229		THERMAL	GND_SMC_AVSS	46 47 50 94
I233		THERMAL	SMC_DIMM_ISENSE	46 50
I235		THERMAL	SMC_DIMM_1V5_R	50
I231		THERMAL	SMC_DIMM_VSENSE	46 50
I228		THERMAL	GND_SMC_AVSS	46 47 50 94
I227		THERMAL	SMC_VCCSA_ISENSE	46 50
I226		THERMAL	SMC_VCCSA_ISENSE_R	50
I225		THERMAL	SMC_VCCSA_VSENSE	46 50
		THERMAL	GND_SMC_AVSS	46 47 50 94
		THERMAL	SMC_PCH_1V05_ISENSE	46 50
		THERMAL	SMC_VAXG_VSENSE	46 50
		THERMAL	SMC_PCH_1V05_VSENSE	46 50
I238		THERMAL	GND_SMC_AVSS	46 47 50 94
I239		THERMAL	SMC_1V05_ISENSE	46 50
I237		THERMAL	SMC_VAXG_ISENSE	46 50
I240		THERMAL	SMC_1V05_VSENSE	46 50
I230		THERMAL	SMC_GPU_ISENSE	46 50
		THERMAL	SMC_GPU_VSENSE	46 50
		THERMAL	SMC_VCORE_ISENSE	46 50
I237		THERMAL	SMC_VCORE_VSENSE	46 50
I230		THERMAL	SMC_CPU_VSENSE	

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NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SWITCHNODE	SWITCHNODE	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	BGA_P1MM	BGA_P2MM
SWITCHNODE	GND	BGA_P1MM	BGA_P2MM
SWITCHNODE	*	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	*	6:1_SPACING
SWITCHNODE	GND	*	6:1_SPACING
SWITCHNODE	*	*	SWITCHNODE

POWER NET PROPERTIES

NET_TYPE PHYSICAL	SPACING	VOLTAGE		
POWER	SWITCHNODE	1.5V	VR_CPU_PHASE1	66
POWER	SWITCHNODE	1.5V	VR_CPU_PHASE2	66
POWER	SWITCHNODE	1.5V	VR_CPU_PHASE3	66
POWER	SWITCHNODE	1.5V	VR_CPU_PHASE4	
POWER	SWITCHNODE	1.5V	VR_AXG_PHASE1	67
POWER	SWITCHNODE	3.3V	P3V3S5_REG_PHASE	70
POWER	SWITCHNODE	5V	P5VS3_REG_PHASE	70
POWER	SWITCHNODE	1.05V	P1V05S0_PHASE	68
POWER	SWITCHNODE	1.05V	P1V05_REG_PHASE	
POWER	SWITCHNODE	3.4V	P3V42G3H_SW	72
POWER	SWITCHNODE	3.3V	ENET_3V3_S3_SR_IN	37
POWER	SWITCHNODE	1.2V	ENET_SR_LX	36 37
POWER	SWITCHNODE	1.5V	DDR_REG_PHASE	71
POWER	SWITCHNODE	1.8V	P1V8_REG_PHASE	71
POWER	POWER	0.75V	PP0V75_S3_MEM_VREFCA_A	28 30
POWER	POWER	0.75V	PP0V75_S3_MEM_VREFCA_B	28 31
POWER	POWER	0.75V	PP0V75_S3_MEM_VREFDQ_A	28 30
POWER	POWER	0.75V	PP0V75_S3_MEM_VREFDQ_B	28 31
POWER	POWER	12V	PP12V_S0	6
POWER	POWER	12V	PP12V_S0_CPU_FLTRD	65 66 67
POWER	POWER	12V	PP12V_S0_FAN0_L	53 98
POWER	POWER	12V	PP12V_S0_FAN1_L	53 98
POWER	POWER	12V	PP12V_S0_FAN2_L	54 98
POWER	POWER	12V	VR_CPU_DRV1_PVCC	66
POWER	POWER	12V	VR_CPU_DRV1_UVCC	66
POWER	POWER	12V	VR_CPU_DRV2_PVCC	66
POWER	POWER	12V	VR_CPU_DRV2_UVCC	66
POWER	POWER	12V	VR_CPU_DRV3_PVCC	66
POWER	POWER	12V	VR_CPU_DRV3_UVCC	66
POWER	POWER	12V	VR_CPU_DRV4_PVCC	
POWER	POWER	12V	VR_CPU_DRV4_UVCC	
POWER	POWER	12V	VR_AXG_DRV1_PVCC	67
POWER	POWER	12V	VR_AXG_DRV1_UVCC	
POWER	POWER	12V	VR_CPU_DRV1_VCC	66
POWER	POWER	12V	VR_CPU_DRV2_VCC	66
POWER	POWER	12V	VR_CPU_DRV3_VCC	66
POWER	POWER	12V	VR_CPU_DRV4_VCC	
POWER	POWER	12V	PP12V_S0_VG_OK	41
POWER	POWER	12V	P12V_FW_R	41
POWER	POWER	12V	P12V_FW_CL	41
POWER	POWER	12V	P12V_FW_D	41
POWER	POWER	12V	FW_PORT0_VP	41
POWER	POWER	12V	FW_PORT0_VP_F	41
POWER	POWER	12V	PPVP_FW_PHY_CPS	39 41
POWER	POWER	12V	PP12V_S0_P1V05_VREG_VIN	68
POWER	POWER	12V	VCCSA_PWR_RC	69
POWER	POWER	12V	PP12V_S0_BL_R	
POWER	POWER	12V	PP12V_S5_FET	6 74
POWER	POWER	12V	PP12V_LCD	81
POWER	POWER	12V	PP12V_G3H	6
POWER	POWER	12V	PP12V_S5	6
POWER	POWER	12V	PP12V_S5_RSN	74
POWER	POWER	0.75V	PPVTT_S0_DDR	6
POWER	POWER	0.75V	PP0V75_S0	6
POWER	POWER	0.925V	PPVCCSA_S0_CPU	6
POWER	POWER	1.0V	PP1V0_FW_FWPHY_AVDD	39
POWER	POWER	1.0V	PP1V0_S0_FW_VDD	40
POWER	POWER	1.05V	PP1V05_S0_T29	6
POWER	POWER	1.05V	PP1V05_S0_INPUT_VCCSA	6
POWER	POWER	1.05V	PPVAXG_S0	6
POWER	POWER	1.05V	PP1V05_S0	6
POWER	POWER	1.05V	PP1V05_S0_PCH	6
POWER	POWER	1.05V	PP1V05_S0_CK505_F	26
POWER	POWER	1.05V	PPVOUT_S5_PCH_DCPSUS	22
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLA_F	17 22
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLB_F	17 22
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_EXP_F	22 24
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLLDMI2_F	22 24
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_SATA_F	22 24
POWER	POWER	1.05V	PP1V05_S0_PCH_VCCCLKDMI_F	22 24
POWER	POWER	1.1V	PPVCORE_S0_AXG_REG1	67
POWER	POWER	1.1V	PPVCORE_S0_AXG_REGOUT	67
POWER	POWER	1.1V	PPVCORE_S0_CPU	6
POWER	POWER	1.1V	PPVCORE_S0_CPU_REG1	66
POWER	POWER	1.1V	PPVCORE_S0_CPU_REG2	66
POWER	POWER	1.1V	PPVCORE_S0_CPU_REG3	66
POWER	POWER	1.1V	PPVCORE_S0_CPU_REG4	
VR_CTL_PHY	VR_CTL	1.2V	PP1V2_S3_ENET_INTREG	36
POWER	POWER	1.2V	PP1V2_S3_ENET_PHY_AVDDL	37
POWER	POWER	1.2V	PP1V2_S3_ENET_PHY_PCIEPLL	37
POWER	POWER	1.2V	PP1V2_S3_ENET_PHY_GPHYPLL	37
POWER	POWER	1.5V	PP1V5_S0	6
POWER	POWER	1.5V	PP1V5_S0_CK505_F	26
POWER	POWER	1.5V	PP1V5_S0_CK505_R	26
POWER	POWER	1.5V	PP1V5_S0_CPU_MEM	6
POWER	POWER	1.5V	PP1V5_S0_CPU_SNS	
POWER	POWER	1.5V	PP1V5_S3	6
POWER	POWER	1.5V	PP1V5_S3_MEM	6

POWER NET PROPERTIES

NET_TYPE PHYSICAL	SPACING	VOLTAGE		
POWER	POWER	12V	PP12V_S0_MXM	6
POWER	POWER	12V	PP12V_SLG1	
POWER	POWER	12V	PP3V3R12V_SW_DPAPWR_1	
POWER	POWER	12V	PP3V3R12V_SW_DPBPWR_1	
POWER	POWER	1.8V	USB_HUB2_VDD1V8	35
POWER	POWER	1.8V	USB_HUB2_VDD1V8PLL	35
POWER	POWER	1.8V	PP1V8_S0	6
POWER	POWER	1.8V	PP1V8R1V5_S0_PCH_VCCVRM_F	22 24
POWER	POWER	1.8V	USB_HUB1_VDD1V8	34
POWER	POWER	1.8V	USB_HUB1_VDD1V8PLL	34
POWER	POWER	1.8V	PP3V3R1V8_ENET_LR_OUT_REG	37
POWER	POWER	3.3V	PPVBAT_G3_SYSCLK_R	79
POWER	POWER	3.3V	USB_HUB1_VDDPLL3V3	34
POWER	POWER	3.3V	USB_HUB1_VDDA3V3	34
POWER	POWER	3.3V	USB_HUB2_VDDPLL3V3	35
POWER	POWER	3.3V	USB_HUB2_VDDA3V3	35
POWER	POWER	3.3V	PP3V3R1V5_PCH_VCCSUSHDA	22 24
POWER	POWER	3.3V	PP3V3_S0_CK505_F	26
POWER	POWER	3.3V	PP3V3_S0_HS_F	62
POWER	POWER	3.3V	PP3V3_S0_SW_SD_PWR	45
POWER	POWER	3.3V	PP3V3_S0_PCH_VCCA_DAC_F	17 22
POWER	POWER	3.3V	PP3V3_S0	6
POWER	POWER	3.3V	PP3V3_SMCUSBMUX	43
POWER	POWER	3.3V	PP3V3_S3	6 98
POWER	POWER	3.3V	PP3V3_S3_BT_FLT	44
POWER	POWER	3.3V	PP3V3_S3_MINI_CONN	33
POWER	POWER	3.3V	PP3V3_S3_SDCARD_FLT	44
POWER	SWITCHNODE	3.3V	PP3V3_S3_ENET_PHY_FET	36
POWER	POWER	3.3V	PP3V3_S3_ENET_PHY_XTALVDDH	37
POWER	POWER	3.3V	PP3V3_S3_ENET_PHY_BIASVDDH	37
POWER	POWER	3.3V	PP3V3_S3_ENET_PHY_AVDDH	37
POWER	POWER	3.3V	ENET_XTALVDDH	37
POWER	POWER	3.3V	PP3V3_S5	6
POWER	POWER	3.3V	PP3V3_S5_REG_R	70
POWER	POWER	3.3V	PPVOUT_S0_PCH_DCPSST	22
POWER	POWER	3.3V	PPVOUT_PCH_DCPSUSBYP	
POWER	POWER	3.3V	PPVOUT_G3_PCH_DCPRTC	22
POWER	POWER	3.3V	PPVBATT_G3_RTC	27
POWER	POWER	3.3V	PPVBATT_G3_RTC_R	27
POWER	POWER	3.3V	PP3V3_AUDIO_SPDIF_JACK	60 98
POWER	POWER	3.3V	PP3V3_FW_FWPHY_VDDA	39
POWER	POWER	3.3V	PP3V3_FW_FWPHY_VP25	39
POWER	POWER	3.3V	PP3V3_S0_T29	6
POWER	POWER	3.3V	PP3V3_SW_DPAPWR	78 84
POWER	POWER	3.3V	PP3V3_SW_DPBPWR	
POWER	POWER	3.3V	PP3V3_G3H_RTC	18 19 22 27
POWER	POWER	3.3V	PP3V3_G3H_AVREF_SMC	46 47
POWER	POWER	3.4V	PP3V3_G3H_SMC_AVCC	46
POWER	POWER	3.42V	PP3V42_G3H	6
POWER	POWER	4.5V	4V5_REG_IN	56
POWER	POWER	4.5V	PP4V5_AUDIO_ANALOG	56 61
POWER	POWER	4.5V	PP5V_AUDIO_HPAMP	56
POWER	POWER	5V	PP5V_LAMP_VREG	56 59
POWER	POWER	5V	PP5V_RAMP_VREG	58
POWER	POWER	5V	PP5V_S0	6 98
POWER	POWER	5V	PP5V_S0_CPU_VCORE_VCC	65
POWER	POWER	5V	PP5V_S0_PCH_V5REF	24
POWER	POWER	5V	PP5V_S0_SATA_FET	42
POWER	POWER	5V	5V_S0_P1V05REG_VIN	68
POWER	POWER	5V	5V_S0_P1V05REG_VDD	68
POWER	POWER	5V	PP5V_S3	6 98
POWER	POWER	5V	PP5V_S3_VREFMRGN_A	28
POWER	POWER	5V	PP5V_S3_VREFMRGN_B	28
POWER	POWER	5V	PP5V_S3_DDR_REG_V5FILT	71
POWER	POWER	5V	PP5V_S3_CAMERA_FLT	44
POWER	POWER	5V	PP5V_S3_REG_R	70
POWER	POWER	5V	PP5V_S3_IR_FLT	44 98
POWER	POWER	5V	PP5V_S5	6
POWER	POWER	5V	PP5V_S5_PCH_V5REFSUS	24
POWER	POWER	5V	PP5V_USB_PORT0	43
POWER	POWER	5V	PP5V_USB_PORT0_F	43
POWER	POWER	5V	PP5V_USB_PORT1	43
POWER	POWER	5V	PP5V_USB_PORT1_F	43
POWER	POWER	5V	PP5V_USB_PORT2	43
POWER	POWER	5V	PP5V_USB_PORT2_F	43
POWER	POWER	5V	PP5V_USB_PORT3	43
POWER	POWER	5V	PP5V_USB_PORT3_F	43
POWER	POWER		DDR_REG_PGND	71
POWER	POWER		DDR_REG_CSGND	71
	POWER	3.3V	PPVDDIO_25M_B	79
	POWER	1.05V	PPVDDIO_25M_A	79
	POWER	3.3V	PPVDDIO_25M_C	79
	POWER	12V	PP3V3R12V_SW_DPAPWR_R	85
	POWER	12V	PP3V3R12V_SW_DPAPWR_D	82
	POWER	1.5V	PP1V5_S0_DP_R	83

SENSING NET PROPERTIES

NET_TYPE PHYSICAL	SPACING		
SNS_DIFF	THERMAL	VR_CPU_ISNS1_P	65 66
SNS_DIFF	THERMAL	VR_CPU_ISNS1_N	65 66
SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_N	65
SNS_DIFF	THERMAL	VR_CPU_ISNS2_P	65 66
SNS_DIFF	THERMAL	VR_CPU_ISNS2_N	65 66
SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_N	65
SNS_DIFF	THERMAL	VR_CPU_ISNS3_P	65 66
SNS_DIFF	THERMAL	VR_CPU_ISNS3_N	65 66
SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_N	65
SNS_DIFF	THERMAL	VR_CPU_ISNS4_P	
SNS_DIFF	THERMAL	VR_CPU_ISNS4_N	
SNS_DIFF	THERMAL	VR_CPU_ISNS4_R_N	
SNS_DIFF	THERMAL	P1V05S0_ISN	68
SNS_DIFF	THERMAL	P1V05S0_ISP	68
SNS_DIFF	THERMAL	VR_AXG_ISNS_R_P	65
SNS_DIFF	THERMAL	VR_AXG_ISNS_R_N	65
SNS_DIFF	THERMAL	VR_AXG_ISNS_N	65 67
SNS_DIFF	THERMAL	VR_AXG_ISNS_P	65 67
SNS_DIFF	THERMAL	VR_ISNS_1V05_N	94
SNS_DIFF	THERMAL	VR_ISNS_1V05_P	94
SNS_DIFF	THERMAL	VR_ISNS_VAXG_N	50 94
SNS_DIFF	THERMAL	VR_ISNS_VAXG_P	50 94
SNS_DIFF	THERMAL	VR_ISNS_VCORE_N	50 94
SNS_DIFF	THERMAL	VR_ISNS_VCORE_P	50 94
SNS_DIFF		CPU_VAXG_SENSE_P	13 65
SNS_DIFF		CPU_VAXG_SENSE_N	13 65
SNS_DIFF		VR_AXG_VSNS_R_N	65
SNS_DIFF		VR_AXG_VSNS_R_P	65
SNS_DIFF		VR_AXG_VSEN	65
SNS_DIFF		VR_AXG_RGND	65
SNS_DIFF		VR_AXG_VSNS_XW_N	65
SNS_DIFF		VR_AXG_VSNS_XW_P	65
SNS_DIFF		CPU_VCC_SENSE_N	13 65
SNS_DIFF		CPU_VCC_SENSE_P	13 65
SNS_DIFF		VR_CPU_VSEN	65
SNS_DIFF		VR_CPU_RGND	65
SNS_DIFF		VR_CPU_VSNS_R_N	65
SNS_DIFF		VR_CPU_VSNS_R_P	65
SNS_DIFF		VR_CPU_VSNS_XW_P	65
SNS_DIFF		VR_CPU_VSNS_XW_N	65
SNS_DIFF		CPU_VCCIO_SENSE_P	13 68
SNS_DIFF		CPU_VCCIO_SENSE_N	13 68
SNS_DIFF		P1V05S0_VSEN	68
SNS_DIFF		P1V05S0_RTN	68

VR CTRL NET PROPERTIES

NET_TYPE PHYSICAL	SPACING		
VR_CTL_PHY	SWITCHNODE	VR_CPU_PH1_SNUB	66
VR_CTL_PHY	SWITCHNODE	VR_CPU_PH2_SNUB	66
VR_CTL_PHY	SWITCHNODE	VR_CPU_PH3_SNUB	66
VR_CTL_PHY	SWITCHNODE	VR_CPU_PH4_SNUB	
VR_CTL_PHY	VR_CTL	VR_CPU_COMP	65
VR_CTL_PHY	VR_CTL	VR_AXG_TM	65
VR_CTL_PHY	VR_CTL	VR_AXG_PWM_R	65
VR_CTL_PHY	VR_CTL	VR_AXG_PWM	65 67
VR_CTL_PHY	VR_CTL	VR_CPU_PWM2	65 66
VR_CTL_PHY	VR_CTL	VR_CPU_PWM1	65 66
VR_CTL_PHY	VR_CTL	VR_CPU_PWM1_R	65
VR_CTL_PHY	VR_CTL	VR_CPU_PWM2_R	65
VR_CTL_PHY	VR_CTL	VR_CPU_PWM3	65 66
VR_CTL_PHY	VR_CTL	VR_CPU_PWM3_R	65
VR_CTL_PHY	VR_CTL	VR_CPU_PWM4	
VR_CTL_PHY	VR_CTL	VR_CPU_PWM4_R	65
VR_CTL_PHY	VR_CTL	VR_AXG_SW_FREQ	65
VR_CTL_PHY	VR_CTL	VR_EN_PWR_OVP	65
VR_CTL_PHY	VR_CTL	VR_RSET	65
VR_CTL_PHY	VR_CTL	VR_EN_PWR_OVP_R	65
VR_CTL_PHY	VR_CONTROL	VR_CPU_BOOT1_RC	66
VR_CTL_PHY	VR_CONTROL	VR_CPU_BOOT2_RC	66
VR_CTL_PHY	VR_CONTROL	VR_CPU_BOOT3_RC	66
VR_CTL_PHY	VR_CONTROL	VR_AXG_BOOT1_RC	67
VR_CTL_PHY	VR_CTL	VR_CPU_BOOT4_RC	
VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV1_BOOT	66
VR_CTL_PHY	VR_CTL	VR_CPU_DRV1_GDSEL	66
VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV1_LGATE	66
VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV1_UGATE	66
VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV2_BOOT	66
VR_CTL_PHY	VR_CTL	VR_CPU_DRV2_GDSEL	66
VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV2_LGATE	66
VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV2_UGATE	66
VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV3_BOOT	66
VR_CTL_PHY	VR_CTL	VR_CPU_DRV3_GDSEL	66
VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV3_LGATE	66
VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV3_UGATE	66
VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV4_BOOT	
VR_CTL_PHY	VR_CTL	VR_CPU_DRV4_GDSEL	
VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV4_LGATE	
VR_CTL_PHY	VR_CONTROL	VR_CPU_DRV4_UGATE	
VR_CTL_PHY	VR_CONTROL	VR_AXG_DRV1_BOOT	67
VR_CTL_PHY	VR_CTL	VR_AXG_DRV1_UGATE_R	67
VR_CTL_PHY	VR_CONTROL	VR_AXG_DRV1_LGATE	67
VR_CTL_PHY	VR_CONTROL	VR_AXG_DRV1_UGATE	67
VR_CTL_PHY	VR_CTL	VR_CPU_SW_FREQ	65
VR_CTL_PHY	VR_CTL	VR_CPU_FB	65
VR_CTL_PHY	VR_CTL	VR_CPU_FB_R	65
VR_CTL_PHY	VR_CTL	VR_CPU_RAMP_ADJ	65
VR_CTL_PHY	VR_CTL	VR_CPU_IMON	50 65
VR_CTL_PHY	VR_CTL	VR_CPU_SUTH	65
VR_CTL_PHY	VR_CTL	VR_CPU_N_PSI	65
VR_CTL_PHY	VR_CTL	VR_CPU_FDVID	65
VR_CTL_PHY	VR_CTL	VR_CPU_PSICOMP	65
VR_CTL_PHY	VR_CTL	VR_CPU_IAUTO	65
VR_CTL_PHY	VR_CTL	VR_CPU_PSICOMP1	65
VR_CTL_PHY	VR_CTL	VR_CPU_PSICOMP2	65
VR_CTL_PHY	VR_CTL	VR_CPU_FB_RC	65
VR_CTL_PHY	VR_CTL	VR_CPU_FB2	65
VR_CTL_PHY	VR_CTL	VR_CPU_IMON_R	65
VR_CTL_PHY	VR_CTL	VR_CPU_HFREQ_COMP	65
VR_CTL_PHY	SWITCHNODE	VR_AXG_PH1_SNUB	67
VR_CTL_PHY	VR_CTL	VR_AXG_IMON	50 65
VR_CTL_PHY	VR_CTL	VR_AXG_IMON_R	65
VR_CTL_PHY	VR_CTL	VR_AXG_HFREQ_COMP	65
VR_CTL_PHY	VR_CTL	VR_AXG_FB	65
VR_CTL_PHY	VR_CTL	VR_SEN_R1	65
VR_CTL_PHY	VR_CTL	VR_SEN_R2	65
VR_CTL_PHY	VR_CTL	VR_SEN_R3	65
VR_CTL_PHY	VR_CTL	VR_AXG_COMP_RC	65
VR_CTL_PHY	VR_CTL	VR_AXG_COMP	65
VR_CTL_PHY	VR_CTL	VR_AXG_TCOMP	65
VR_CTL_PHY	SWITCHNODE	P1V05S0_UGATE	68
VR_CTL_PHY	SWITCHNODE	P1V05S0_LGATE	68
VR_CTL_PHY	VR_CTL	P1V05S0_BOOT	68
VR_CTL_PHY	VR_CTL	P1V05S0_BOOT_R	68
VR_CTL_PHY	VR_CTL	P1V05_IMON	50 68
VR_CTL_PHY	VR_CTL	P1V05S0_FB	68
VR_CTL_PHY	VR_CTL	P1V05S0_PHASE_L	68
VR_CTL_PHY	VR_CTL	P1V05S0_VW	68
VR_CTL_PHY	VR_CTL	P1V05S0_COMP	68
VR_CTL_PHY	VR_CTL	P1V05S0_ICOMP	68
VR_CTL_PHY	VR_CTL	P1V05_S0_VDIFF	68
VR_CTL_PHY	VR_CTL	P1V05S0_COMP_C	68
VR_CTL_PHY	VR_CTL	P1V05S0_VDIF_C	68
VR_CTL_PHY	VR_CTL	P1V05S0_VO	68
VR_CTL_PHY	VR_CTL	P1V05S0_OCSET	68
VR_CTL_PHY	VR_CTL	P1V05S0_SNUBBER	68
VR_CTL_PHY	VR_CTL	P1V05_REG_VFB	
VR_CTL_PHY	VR_CTL	ENET_SR_VFB	36 37
VR_CTL_PHY	VR_CTL	P1V05S0_ISP_R	68
VR_CTL_PHY	VR_CTL	VCCSA_CNTRL_INPUT2_R	69 95
VR_CTL_PHY	VR_CTL	T29BST_FBX	
VR_CTL_PHY	VR_CTL	P3V42G3H_BOOST	72
VR_CTL_PHY	VR_CTL	P3V42G3H_FB	72

VR CTRL NET PROPERTIES

NET_TYPE PHYSICAL	SPACING		
VR_CTL_PHY	VR_CTL	DDR_REG_CS	71
VR_CTL_PHY	VR_CTL	DDR_REG_FB	71
VR_CTL_PHY	VR_CONTROL	DDR_REG_LGATE	71
VR_CTL_PHY	VR_CONTROL	DDR_REG_UGATE	71
VR_CTL_PHY	VR_CONTROL	DDR_REG_BOOT	71
VR_CTL_PHY	VR_CONTROL	DDR_REG_BOOT_R	71
VR_CTL_PHY	VR_CTL	DDR_REG_VDDQSNS	71
VR_CTL_PHY	VR_CTL	DDR_REG_VTTSNS	71
VR_CTL_PHY	VR_CTL	DDR_REG_PHASE_R	71
VR_CTL_PHY	VR_CTL	DDR_REG_UGATE_R	71
VR_CTL_PHY	SWITCHNODE	1V5_SNUBBER	71
VR_CTL_PHY	VR_CTL	P1V8_REG_VFB	71
VR_CTL_PHY	VR_CTL	P1V8_REG_SYNC	71
VR_CTL_PHY	VR_CONTROL	P3V3S5_REG_BOOT	70
VR_CTL_PHY	VR_CONTROL	P3V3S5_REG_BOOT_R	70
VR_CTL_PHY	VR_CTL	P3V3S5_REG_FB	70
VR_CTL_PHY	VR_CTL	P3V3S5_REG_ISEN	70
VR_CTL_PHY	VR_CONTROL	P3V3S5_REG_LGATE	70
VR_CTL_PHY	VR_CTL	P3V3S5_REG_OCSET	70
VR_CTL_PHY	VR_CONTROL	P3V3S5_REG_VOUT1	70
VR_CTL_PHY	VR_CONTROL	P3V3S5_REG_FSET1	70
VR_CTL_PHY	VR_CONTROL	P3V3S5_REG_UGATE	70
VR_CTL_PHY	VR_CTL	P3V3S5_REG_SNUB	70
VR_CTL_PHY	VR_CONTROL	P5VS3_REG_BOOT	70
VR_CTL_PHY	VR_CTL	P5VS3_REG_FB	70
VR_CTL_PHY	VR_CTL	P5VS3_REG_ISEN	70
VR_CTL_PHY	VR_CONTROL	P5VS3_REG_LGATE	70
VR_CTL_PHY	VR_CTL	P5VS3_REG_OCSET	70
VR_CTL_PHY	VR_CTL	P5VS3_REG_FSET2	70
VR_CTL_PHY	VR_CONTROL	P5VS3_REG_UGATE	70
VR_CTL_PHY	VR_CONTROL	P5VS3_REG_VOUT2	70
VR_CTL_PHY	VR_CTL	VCCSA_CNTRL_INPUT1	69
VR_CTL_PHY	VR_CTL	VCCSA_CNTRL_INPUT2	69
VR_CTL_PHY	VR_CTL	VCCSA_CNTRL_INPUT2_R	69 95
VR_CTL_PHY	VR_CTL	VCCSA_OUT	69
VR_CTL_PHY	VR_CTL	VCCSA_GATE	69
VR_CTL_PHY	VR_CTL	VCCSA_REF	69
VR_CTL_PHY	VR_CTL	VCCSA_CRL	69
VR_CTL_PHY	VR_CTL	CPU_VCCSA_SENSE	13 69
VR_CTL_PHY	VR_CTL	VR_CPU_TM	65
VR_CTL_PHY	PM	3V3R2V9_DPAPWR_ADJ	82 97

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VID_PHY	*	50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL	*	0.35MM	?

VR VID NET PROPERTIES

NET_TYPE PHYSICAL	SPACING		
VID_PHY	VR_CTL_VIDS	CPU_VIDSCLK_R	13
VID_PHY	VR_CTL_VIDS	CPU_VIDALERT_L_R	13
VID_PHY	VR_CTL_VIDS	CPU_VIDSOUT_R	13
VID_PHY	VR_CTL_VIDS	CPU_VIDSCLK	13 65
VID_PHY	VR_CTL_VIDS	CPU_VIDALERT_L	13 65
VID_PHY	VR_CTL_VIDS	CPU_VIDSOUT	13 65

PULL-UP STUB < 1-INCH
VID LENGTH SKEW < 1-INCH
VID LENGTH RANGE< 1 TO 15-INCH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL_VIDS	*	=4X_DIELECTRIC	?

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POWER CONSTRAINTS

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T29 ELECTRICAL ROUTES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29	*	=5X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29	TOP,BOTTOM	=7X_DIELECTRIC	?

T29 PCI-EXPRESS (SAME RULE AS PCIE)

T29 SPI INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	0.2 MM	?

T29 XTAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_XTAL_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_XTAL	*	=4X_DIELECTRIC	?

T29 SMBUS INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SMB	*	=2x_DIELECTRIC	?

GREEN CLOCK CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_25M	*	=5X_DIELECTRIC	?

T29 BIAS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_COMP	*	0.2 MM	?

T29 NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
NO_TEST=TRUE	T29_90D	T29	T29_R2D_C_P<3..0>	78 84 86
NO_TEST=TRUE	T29_90D	T29	T29_R2D_C_N<3..0>	78 84 86
NO_TEST=TRUE	T29_90D	T29	T29_D2R_C_P<3..0>	84 85
NO_TEST=TRUE	T29_90D	T29	T29_D2R_C_N<3..0>	84 85
NO_TEST=TRUE	T29_90D	T29	T29_R2D_P<3..0>	84
NO_TEST=TRUE	T29_90D	T29	T29_R2D_N<3..0>	84
NO_TEST=TRUE	T29_90D	T29	T29_D2R_P<3..0>	78 84 86
NO_TEST=TRUE	T29_90D	T29	T29_D2R_N<3..0>	78 84 86
NO_TEST=TRUE	T29_90D	T29	T29_R2D_C_F_P<3..0>	84
NO_TEST=TRUE	T29_90D	T29	T29_R2D_C_F_N<3..0>	84
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_P<3..0>	84 85
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_N<3..0>	84 85
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_P<3..0>	
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_N<3..0>	
NO_TEST=TRUE	T29_90D	T29	DP_A_EXT_AUXCH_P	84 85
NO_TEST=TRUE	T29_90D	T29	DP_A_EXT_AUXCH_N	84 85
NO_TEST=TRUE	T29_90D	T29	DP_SDRVA_AUXCH_C_P	84
NO_TEST=TRUE	T29_90D	T29	DP_SDRVA_AUXCH_C_N	84
NO_TEST=TRUE	T29_90D	T29	DP_SDRVB_AUXCH_C_P	
NO_TEST=TRUE	T29_90D	T29	DP_SDRVB_AUXCH_C_N	
NO_TEST=TRUE	T29_90D	T29	DP_B_EXT_AUXCH_P	
NO_TEST=TRUE	T29_90D	T29	DP_B_EXT_AUXCH_N	
NO_TEST=TRUE	T29_90D	T29	T29DPA_D2R1_AUXCH_P	85
NO_TEST=TRUE	T29_90D	T29	T29DPA_D2R1_AUXCH_N	85
NO_TEST=TRUE	T29_90D	T29	T29DPB_D2R3_AUXCH_P	
NO_TEST=TRUE	T29_90D	T29	T29DPB_D2R3_AUXCH_N	
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_C_N<0>	84 85
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_C_P<0>	84 85
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_C_N<2>	84 85
NO_TEST=TRUE	T29_90D	T29	T29DPA_ML_C_P<2>	84 85
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_C_N<0>	
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_C_P<0>	
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_C_N<2>	
NO_TEST=TRUE	T29_90D	T29	T29DPB_ML_C_P<2>	
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_R2D_P<3..0>	86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_R2D_N<3..0>	86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_R2D_C_P<3..0>	18 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_R2D_C_N<3..0>	18 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_D2R_P<3..0>	18 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_D2R_N<3..0>	18 86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_D2R_C_P<3..0>	86
NO_TEST=TRUE	PCIE_85D	PCIE	PCIE_T29_D2R_C_N<3..0>	86
NO_TEST=TRUE	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P	18 86
NO_TEST=TRUE	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N	18 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_P<3..0>	83
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_N<3..0>	83
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_ML_P<3..0>	83 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_ML_N<3..0>	83 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_P<3..0>	86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_N<3..0>	86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_P	86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_N	86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0>	78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0>	78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P	78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N	78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_P<3..0>	86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_N<3..0>	86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_P	86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_N	86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0>	78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0>	78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P	78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N	78 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_R_C_P	83
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_R_C_N	83
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_P	83 86
NO_TEST=TRUE	DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_N	83 86
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_AUXCH_P	84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_AUXCH_N	84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_AUXCH_P	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_AUXCH_N	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_C_P<3..0>	84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_C_N<3..0>	84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_P<3..0>	84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_N<3..0>	84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_R_P<3..0>	84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVA_ML_R_N<3..0>	84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_C_P<3..0>	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_C_N<3..0>	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_P<3..0>	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_N<3..0>	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_R_P<3..0>	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	DP_SDRVB_ML_R_N<3..0>	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29_A_RSVD_N	84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29_A_RSVD_P	84
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29_B_RSVD_N	
NO_TEST=TRUE	T29_90D	DISPLAYPORT	T29_B_RSVD_P	

T29 NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	T29_SPI_55S	T29_SPI	JTAG_T29_TDI	15 21 86
	T29_SPI_55S	T29_SPI	JTAG_T29_TMS	15 18 86
	T29_SPI_55S	T29_SPI	JTAG_T29_TCK	15 21 25 86
	T29_SPI_55S	T29_SPI	JTAG_T29_TDO	15 21 86
I43J	T29_SPI_55S	T29_SPI	T29_SPI_MOSI	86
I43H	T29_SPI_55S	T29_SPI	T29_SPI_MISO	86
I43G	T29_SPI_55S	T29_SPI	T29_SPI_CS_L	86
I44D	T29_SPI_55S	T29_SPI	T29_SPI_CLK	86
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29	79 86 96
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_R	86 96
	T29_SMB_55S	T29_SMB	I2C_T29_SDA	49 86
	T29_SMB_55S	T29_SMB	I2C_T29_SCL	49 86
I42I	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB	79
I42J	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET	79
I42G	CLK_25M_55S	CLK_25M	ENET_CLK25M_XTALI_OSC	36 79
I42G	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_CLK	79
I43J	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29	79 86 96
I42H	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_R	86 96
I42C	T29_XTAL_100D	T29_XTAL	SYSCLK_CLK25M_X2	79
I42D	T29_XTAL_100D	T29_XTAL	SYSCLK_CLK25M_X2_R	79
I42F	T29_XTAL_100D	T29_XTAL	SYSCLK_CLK25M_X1	79
I43I	T29_55S	T29_COMP	T29_RSENSE	86
I43J	T29_55S	T29_COMP	T29_RBIAS	86
I43E		T29_COMP	T29_A_BIAS	82 84 85
I43E		T29_COMP	T29_B_BIAS	
I43E		T29_COMP	DP_A_BIAS	84

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PM NET PROPERTIES
(PM, RESET, EN, PGOOD)

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PM	*	*	2:1_SPACING
PM_VTT	PM_VTT	*	2:1_SPACING
PM_VTT	*	*	3:1_SPACING
PM_VTT	GND	*	DEFAULT
PM	GND	*	DEFAULT

PHYSICAL	NET_TYPE SPACING		
I357	PM	4V5_REG_EN	56
I358	PM	3V42G3H_SHDN_L	72
I359	PM	ALL_SYS_PWRGD_R	5 32 64
I360	PM	ALL_SYS_PWRGD_SMC	46 64
I361	PM	AP_PWR_EN	20 25 33
I362	PM	AP_MINI_RESET_L	33
I363	PM	AUD_I2C_INT_L	20 62
I364	PM	AUD_IP_PERIPHERAL_DET	20 61
I365	PM	AUD_IPHS_SWITCH_EN	21 62
I366	PM	AUD_SPDIF_IN	60 83 91
I367	PM	AUD_SPDIF_IN_CODEC	56 83
I368	PM	BDV_BKL_PWM	46 83 97
I369	PM	BL_PWM	6 83
I370	PM	BL_EN	6 81
I371	PM	BDV_BKL_PWM	46 83 97
I372	PM	CK505_27MHZ_EN	26
I373	PM	CPUVTT_REG_EN	
I374	PM_VTT	CPUVTT_REG_PGOOD_R	63
I375	PM	CPU_MEM_RESET_L	11 32
I376	PM	CPU_PECI_R	46
I377	PM_VTT	CPU_PWRGD	11 21 25
I378	PM	CPU_RESET_L	11 27
I379	PM	CPU_SKTOCC_L	11 63
I380	PM	CPU_CATERR_L	11
I381	PM	CPU_PECI	11 21 46
I382	PM	CPU_PROCHOT_L	11 47 65
I383	PM	CPU_THRMTRIP_L	11 47
I384	PM	CPU_PROC_SEL	11 19
I385	PM	DEBUG_RESET_L	27 48
I386	PM	DDRVTT_EN	
I387	PM	DP_INT_SPDIF_AUDIO	81 83
I388	PM	DP_INTPNL_HPD	81 83
I389	PM	3V3R2V9_DPAPWR_ADJ	82 95
I390	PM	DP_A_PWRDWN	84
I391	PM	DP_A_PWRDWN_FET_R	82
I392	PM	DP_A_PWRDWN_INV	82
I393	PM	DPAPWRSW_HVEN_L_R	82
I394	PM	DPAPWRSW_CT	82
I395	PM	DPAPWRSW_ILIM	82
I396	PM	DPAPWRSW_IFLT	82
I397	PM	T29_A_HV_EN	82 84
I398	PM	3V3R2V9_DPBPWR_ADJ	
I399	PM	DP_B_PWRDWN	
I400	PM	DP_B_PWRDWN_FET_R	
I401	PM	DP_B_PWRDWN_INV	
I402	PM	DPBPWRSW_HVEN_L_R	
I403	PM	DPBPWRSW_CT	
I404	PM	DPBPWRSW_ILIM	
I405	PM	DPBPWRSW_IFLT	
I406	PM	T29_B_HV_EN	
I407	PM	T29_PWR_EN	18 80 97
I408	PM	T29_RESET_RTR_L	80 86
I409	PM	LCD_BL_FILT	83
I410	PM	LCD_BLK_ON_DLY	
I411	PM	LCD_BL_PWM	83
I412	PM	MXM_PNL_BL_PWM	76 83

PHYSICAL	NET_TYPE SPACING		
I225	PM	ENET_PWR_EN	20 25 36
I227	PM	ENET_LOW_PWR	15 21 37
I229	PM	FW_RESET_L	27 39
I231	PM	ENET_RESET_L	27 36
I233	PM	FW_PME_L	15 21 39
I234	PM	FW_PWR_EN	15 21
I235	PM	FW_CLKREQ_L	15 39
I248	PM	ISOLATE_CPU_MEM_L	21 25 32
I266	PM	LPC_PWRDWN_L	19 46 48
I268	PM	MEM_RESET_L	30 31 32 89
I269	PM	MINI_CLKREQ_L	15 33
I270	PM	MINI_RESET_L	27 33
I271	PM	MXM_CLKREQ_L	9 75
I272	PM	MXM_GOOD	5 21 25
I273	PM	ODD_PWR_EN_L	15 21 42
I68	PM	RTC_RESET_L	18 27 97
I48	PM	RSMRST_PWRGD	46 64
I57	PM	RTC_RESET_L	18 27 97
I810	PM	S4_ENABLES	63
I268	PM	SDCONN_STATE_RST_L	
I269	PM	SDCONN_DETECT_BUF_L	92
I270	PM	SDCONN_STATE_CHANGE	20 25 45
I271	PM	SDCARD_RESET	15 21 44 98
I814	PM	SDCARD_RESET_L	44
I816	PM	SDCARD_PLT_RST_L	27 44
I856	PM	SDCARD_PLT_RST_L_R	
I815	PM	SMC_PM_G2_EN	46 74
I852	PM	SMC_PM_G2_EN_R	74
I853	PM	SMC_PM_G2_EN_L	74
I855	PM	S5_DG_1	74
I854	PM	S5_MSFT_G1	74
I415	PM	USE_HDD_OOB_L	20 51
I416	PM	HDD_OOB_1V00_REF	51
I418	PM	SMC_ADAPTER_EN	19 46 47
I419	PM	SMC_RUNTIME_SCI_L	21 46 47
I420	PM	SMC_WAKE_SCI_L	15 18 21 46
I421	PM	SMC_DELAYED_PWRGD	47 64
I422	PM	SMC_LRESET_L	27 46
I423	PM	SMC_RESET_L	46 47 48
I424	PM	SMC_PROCHOT	46 47
I425	PM	SMC_PROCHOT_3_3_L	46 47
I426	PM	SMC_ONOFF_L	46 47
I427	PM	SMC_MANUAL_RST_L	47
I428	PM	SPI_DESCRIPTOR_OVERRIDE_L	18 46
I415	PM	T29_PWR_EN	18 80 97
I416	PM	T29_RESET_L	27 80
I418	PM	T29_DP_PORTA_PWR_EN	20 25 82 91
I419	PM	T29_DP_PORTA_PWR_EN_REG	82
I420	PM_VTT	XDP_CPUPWRGD	
I421	PM_VTT	XDP_DBRESET_L	11 25
I422	PM_VTT	XDP_PWRGD	
I423	PM	XDPPCH_PLTRST_L	25 27
I424	PM	USB_HUB_SOFT_RESET_L	20 25 34
I182	PM	VSYNC_DP_CONN	6 81
I182	PM	VSYNC_DP	81
I182	PM	VIDEO_ON	81
I844	PM	VTT_REG_PGOOD_L	63

PHYSICAL	NET_TYPE SPACING		
I272	PM	PLT_RESET_L	20 27
I472	PM_VTT	PLT_RESET_LS1V05_L	11
I274	PM	PM_BATLOW_L	15 19 46
I275	PM	PM_CLK32K_SUSCLK	9 46 91
I275	PM	PM_CLK32K_SUSCLK_R	9 19 91
I277	PM	PM_CLKRUN_L	15 19 46 48
I278	PM	PM_PWRBTN_L	19 25 46
I279	PM	PM_RSMRST_L	27 46
I276	PM	PM_RSMRST_PCH_L	19 27
I138	PM	PCH_SRTCRST_L	18
I137	PM	PCH_INTVRMEN_L	18
I141	PM	PCH_DSWVRMEN	19
I139	PM	PCH_DF_TVS	19
I152	PM	PCH_PROCPWRGD	21
I143	PM	PCIE_WAKE_L	19 33 36 78
I142	PM	PM_DSW_PWRGD	19
I145	PM	PM_ASW_PWRGD	19 64
I146	PM	PM_MEM_PWRGD_R	11
I150	PM	PM_EN_DDR1V5_S3_REG	63 71
I147	PM	PM_EN_DDRVTT_S0_REG	32 63 71
I160	PM	PM_EN_P12V_S0_FET	6 63
I169	PM	PM_EN_P1V05_S0_REG	63 68
I170	PM	PM_EN_P1V05_S3_REG	
I171	PM	PM_EN_P1V5_S0_FET	63 73
I172	PM	PM_EN_P1V8_S0_REG	63 71
I173	PM	PM_EN_P3V3_S0_FET	63 73
I174	PM	PM_EN_P3V3_S3_FET	63 73
I175	PM	PM_EN_P3V3_S5_REG	70
I176	PM	PM_EN_P5V_S0_FET	63 73
I177	PM	PM_EN_P5V_S3_REG	63 70
I178	PM	PM_EN_PVCCSA_S0_REG_L	64
I179	PM	PM_EN_VCCSA_S0_CPU	
I179	PM	PM_EN_PVCORE_CPU	63 65
I180	PM_VTT	PM_MEM_PWRGD	11 19 97
I181	PM	PM_MXM_EN	64 76
I182	PM	PM_PCH_PWRGD_R	64
I183	PM	PM_PECI_PWRGD	46 64
I185	PM	PM_PECI_PWRGD_R	46
I186	PM	PM_PGOOD_DDR1V5_S3_REG	5 63 71
I187	PM	PM_PGOOD_P1V05_S0_REG	63 64 68
I188	PM	PM_PGOOD_P1V5_S0_FET	11 64 73
I189	PM	PM_PGOOD_P1V8_S0_REG	64 71
I190	PM	PM_PGOOD_P3V3_S0_FET	63 64 73
I191	PM	PM_PGOOD_P3V3_S3_FET	34 73
I192	PM	PM_PGOOD_P3V3_S5_REG	27 64 70
I193	PM	PM_PGOOD_P5V_S0_FET	63 64 73
I194	PM	PM_PGOOD_MINI	33
I195	PM	PM_PGOOD_PVCORE_CPU	5 25 64 65
I196	PM	PM_PGOOD_PVCCSA_S0_REG	63 64
I197	PM	PM_PGOOD_P5V_S3_REG	63 70 82
I198	PM	PM_PGOOD_PVAXG	5 65
I257	PM_VTT	PM_MEM_PWRGD	11 19 97
I144	PM	PM_MEM_PWRGD_L	11
I256	PM	PM_MXM_PGOOD	64 76
I258	PM	PM_PCH_PWRGD	19 21 64
I292	PM	PM_SLP_S3_5V	32
I293	PM	PM_SLP_S3_5V_L	32
I294	PM	PM_SLP_S3_5V_R2	32
I295	PM	PM_SLP_S3_L	5 19 26 32 36 46 47 63 82
I296	PM	PM_SLP_S4_L	5 19 32 46 47 63 97
I298	PM	PM_SLP_S5_L	5 19 46 47 63
I297	PM_VTT	PM_SYNC	11 19
I299	PM	PM_SYSRST_L	19 25 27 46
I300	PM	PM_SYS_PWRGD	19 32 64
I301	PM_VTT	PM_THRMTRIP_L	21 47
I302	PM	PM_SLP_S3_BUF_L	63
I303	PM	PM_SLP_S4_1_L_R	63
I304	PM	PM_SLP_S4_D_L	32
I305	PM	PM_SLP_S4_L	5 19 32 46 47 63 97
I348	PM	PGOOD_P1V5_S0_DLY	11
I349	PM	PGOOD_1V8_S0_G1	64
I350	PM	PGOOD_1V8_S0_G2	64
I400	PM	PGOOD_P12V_S0	63 64
I310	PM	PGOOD_P1V8_S0	64
I311	PM	PGOOD_PCH_S0	5 64
I349	PM	PGOOD_PCH_S0_R	64 91
I312	PM	PGOOD_SYSPWROK	64
I313	PM	PGOOD_SYSPWROK_R	64
I314	PM	POWER_BUTTON_L	47
I315	PM	PEG_RESET_L	9 27
I431	PM	PGOOD_CPU_S0	64
I432	PM	PGOOD_CPU_UNCORE	64 91
I433	PM	PGOOD_5V_1V05_3V3	64 91
I434	PM	PGOOD_3V3_1V05	64 91
I435	PM	PGOOD_12V_S0_G1	64
I437	PM	PGOOD_12V_S0_G2	64
I422	PM	9V_COMP_REF	64
I426	PM	12V_COMP_REF	64
I440	PM	ALL_SYS_PWRGD	64 91

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FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

J4700 USB CAMERA

95 6 IN PP5V_S3 FUNC_TEST=TRUE MIN_ALLOWED_TPS=1
92 44 IN USB_CAMERA_L_P FUNC_TEST=TRUE
92 44 IN USB_CAMERA_L_N FUNC_TEST=TRUE
92 44 IN USB_BT_L_P FUNC_TEST=TRUE
92 44 IN USB_BT_L_N FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4700
1 PP3V3_S3 TESTPOINT NEAR J4700
6 GROUND TESTPOINTS NEAR J4700

J4750 USB CARD READER

97 44 21 15 IN SDCARD_RESET FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4750
2 Ground Testpoints near J4750

J4780 IR BOARD

92 44 IN USB_IR_L_P FUNC_TEST=TRUE
92 44 IN USB_IR_L_N FUNC_TEST=TRUE
95 44 IN PP5V_S3_IR_FLT FUNC_TEST=TRUE

1 GROUND TESTPOINT NEAR J4780

J4520 SATA ODD (HIGH SPEED)

46 42 IN SMC_ODD_DETECT FUNC_TEST=TRUE

1 PP5V_S0 Testpoint near J4520
1 GROUND TESTPOINTS NEAR J4520

J5551 ODD TEMP SENSOR

94 52 IN SNS_ODD_P FUNC_TEST=TRUE
94 52 IN SNS_ODD_N FUNC_TEST=TRUE

J5600 ODD FAN

53 IN FAN_0_PWR_L FUNC_TEST=TRUE
53 IN FAN_TACH0_L FUNC_TEST=TRUE
95 53 IN PP12V_S0_FAN0_L FUNC_TEST=TRUE
53 IN FAN_0_GND FUNC_TEST=TRUE

J5700 CPU FAN

54 IN FAN_2_PWR_L FUNC_TEST=TRUE
54 IN FAN_TACH2_L FUNC_TEST=TRUE
95 54 IN PP12V_S0_FAN2_L FUNC_TEST=TRUE
54 IN FAN_2_GND FUNC_TEST=TRUE
94 54 52 IN SNS_AMB_P FUNC_TEST=TRUE
94 54 52 IN SNS_AMB_N FUNC_TEST=TRUE

1 GROUND TESTPOINT NEAR J5700

J5601 HD FAN

53 IN FAN_1_PWR_L FUNC_TEST=TRUE
53 IN FAN_TACH1_L FUNC_TEST=TRUE
95 53 IN PP12V_S0_FAN1_L FUNC_TEST=TRUE
53 IN FAN_1_GND FUNC_TEST=TRUE

J5400 HDD TEMP SENSOR

94 51 42 IN HDD_OOB_TEMP_FILT FUNC_TEST=TRUE

1 GROUND TESTPOINTS NEAR J5400

J5560 SKIN TEMP SENSOR

94 52 44 IN SNS_SKIN_LEFT_P FUNC_TEST=TRUE
94 52 44 IN SNS_SKIN_LEFT_N FUNC_TEST=TRUE
94 52 IN SNS_SKIN_RIGHT_P FUNC_TEST=TRUE
94 52 IN SNS_SKIN_RIGHT_N FUNC_TEST=TRUE

J6602 AUDIO RIGHT SPEAKER

91 IN AUD_SPKR_OUTLO2R_POUT FUNC_TEST=TRUE
91 IN AUD_SPKR_OUTLO2R_NOUT FUNC_TEST=TRUE
91 IN AUD_SPKR_OUTLO1R_POUT FUNC_TEST=TRUE
91 IN AUD_SPKR_OUTLO1R_NOUT FUNC_TEST=TRUE

J6603 AUDIO LEFT SPEAKER

91 IN AUD_SPKR_OUTLO2L_POUT FUNC_TEST=TRUE
91 IN AUD_SPKR_OUTLO2L_NOUT FUNC_TEST=TRUE
91 IN AUD_SPKR_OUTLO1L_POUT FUNC_TEST=TRUE
91 IN AUD_SPKR_OUTLO1L_NOUT FUNC_TEST=TRUE

J6600 AUDIO AUXILIARY CONNECTOR

2 TP'S

95 60 IN PP3V3_AUDIO_SPDIF_JACK FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
60 IN AUD_LI_DET_JACK FUNC_TEST=TRUE
60 IN AUD_LI_R_JACK FUNC_TEST=TRUE
60 IN AUD_LI_GND_JACK FUNC_TEST=TRUE
60 IN AUD_LI_L_JACK FUNC_TEST=TRUE
60 IN HS_MIC_HI_JACK FUNC_TEST=TRUE
60 IN AUD_HP_L_JACK FUNC_TEST=TRUE
60 IN AUD_HP_GND_JACK FUNC_TEST=TRUE
60 IN AUD_HP_R_JACK FUNC_TEST=TRUE
60 IN AUD_HP_TYPEDET_JACK FUNC_TEST=TRUE
60 IN AUD_IP_PERPH_JACK FUNC_TEST=TRUE
60 IN AUD_HP_TIPDET_JACK FUNC_TEST=TRUE
60 IN AUD_SPDIFIN_JACK FUNC_TEST=TRUE

4 GROUND TESTPOINTS NEAR J6600

GND 17 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=17
95 6 IN PP3V3_S3 2 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
95 6 IN PP5V_S0 FUNC_TEST=TRUE MIN_ALLOWED_TPS=1

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